Analog-to-Digital Conversion for SONET OC-192

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ABSTRACT

In this work, the implementation of a High speed analog-to-digital converter (ADC) for SONET OC-192 is discussed. Following a system level analysis, it is shown that in CMOS technology the sample and hold circuit represents one of the main bottlenecks for implementing an ADC for this application. To satisfy SONET requirements a CMOS sample and hold circuit is proposed that can be used to implement a 6 bit 10 GS/s interleaved ADC.

I. INTRODUCTION

Optical signals propagating through optical fibers suffer from polarization mode dispersion (PMD) due to geometric irregularities of fiber core or internal stresses. (PMD) is one of the main barriers to high data rate long haul communications since it results in pulse broadening and, hence, inter-symbol interference [1]. Several approaches for PMD mitigation were explored, mainly based on optical domain. However, these methods are bulky and expensive [2]. Electronic PMD equalization is an attractive solution, because of its potential for a compact and cost effective implementation. Also it would represent a major step towards implementing the whole optical receiver on a single chip. Several analog equalizers were reported [1], but they did not deliver the performance expected [2]. The main challenge to the implementation of robust digital equalizers to mitigate PMD is building a high speed analog to digital converter that can meet SONET OC-192 requirements. In this paper the implementation of this analog to digital converter in 0.13μm CMOS technology is studied, highlighting the main implementation challenges. Also a sample and hold circuit is proposed to satisfy the performance requirements imposed by SONET OC-192. CMOS technology is selected, because it is the best technology for System-On-Chip as both analog and digital circuits can be efficiently implemented using CMOS.

The conventional optical communication receiver is shown in Fig.1. The photodiode (PD) generates an output current proportional to the received signal power. This current is amplified by the transimpedance amplifier (TIA). The AGC adjusts the gain of the TIA to allow wide range of received signal power. The signal is further amplified by the limiting amplifier and is then fed to the clock and data recovery (CDR) circuitry for data and clock extraction. Equalization can only be carried out before the received signal linearity is altered by the limiting amplifier. Therefore the ADC and the digital equalizer must be inserted after the TIA as shown in Fig.2 [3]. The required specifications for this ADC are derived from SONET OC-192 requirements in the Section II. While in section III, the ADC implementation challenges are discussed. A CMOS sample and hold circuit that can achieve performance dictated by SONET OC-192 is proposed in Section IV. The paper concludes in Section V.

II. SYSTEM ANALYSIS AND ADC SPECIFICATIONS

The first step is to derive the required resolution (number of bits) for the ADC. For OC-192 the bit error rate (BER) should be kept below 10^-12. For binary modulation and assuming a Gaussian distribution for the noise amplitude with zero mean, the probability of error (Pe) is given by

$$ P_e = Q(\sqrt{SNR}) , \text{ where } Q(x) = \frac{1}{\sqrt{2\pi}} \int_{x}^{\infty} e^{-\frac{u^2}{2}} du $$

where SNR is the signal to noise ratio at the decision making device input. For the receiver in Fig.1, the SNR at the output of the TIA needed for 10^-12 BER is 49 (17 dB). This SNR should be preserved in the receiver of Fig.2 so as not to degrade the performance. That is to say the quantization noise introduced by the ADC should be much less than the input noise to the ADC. Since the quantization noise and input noise are uncorrelated they can be directly added. Therefore

$$ SNR_{out} = \frac{S_i}{N_i + N_q} = \frac{1}{S_i/N_i + 1/S_i/N_q} $$

where $S_i$ is the signal to noise power, $N_i$ is the input noise power and $N_q$ is the quantization noise power.

Assuming an input sinusoidal signal of peak to peak voltage equal to full scale voltage

$$ SNR_{out} = \frac{1}{\frac{1}{S_i/N_i} + \frac{1}{S_i/N_q} + \frac{1}{49 + \frac{3}{2}2^N}} $$

where $N$ is the number of bits

1 SONET is a standard that defines a synchronous frame structure for sending multiplexed digital traffic over optical fiber links in North America. The data rate of SONET OC-192 is 10GS/s

2 The input to the limiting amplifier is an analog signal and its output is a saturated digital signal, therefore it is considered as the decision making device.
Eq. (3) is plotted in Fig. 3, which shows that for N greater than 5, the rate of increase of SNRout with N drops significantly. Increasing N from 5 to 6 bits causes less than a 0.5 dB increase in the output signal-to-noise ratio. Therefore, an effective number of bits (ENOB) = 5 is enough for this application. In this analysis, an ADC with N = 6 will be assumed and ENOB ≥ 5 will be targeted.

Sampling clock jitter is a main source of noise to the output signal of high-speed ADC’s and so must be kept below a certain value. The effect of clock jitter is shown conceptually in Fig. 4, where it is assumed that the received signal can be approximated with a sine wave at half the symbol rate (5 GHz). This is the case of a “101010” pattern with the high frequency edges attenuated due to the low pass behaviour of the TIA. Since the ADC is followed by a CDR circuit, the sampling instant would be synchronized with the input data and therefore the signal is sampled at its peak. From Fig. 4, the peak-to-peak voltage noise generated due to clock jitter (Vjitter-p) can be calculated as [4]

\[
\frac{V_{jitter-p}}{V_{pp}} = \frac{1}{2} \left( 1 - \cos \left( \frac{2\pi f_{jitter-p}}{f_b} \right) \right) = \frac{1}{4} \left( 1 - \frac{2\pi f_{jitter-p}}{f_b} \right)^2
\]

where \(V_{pp}\) is the peak-to-peak value of the input signal, \(f_b\) is the bit period and \(f_{jitter-p}\) is the sampling clock peak to peak jitter. If half of the voltage noise is budgeted for timing noise and half for other sources of noise and assuming that half of timing error is due to transmitter and half due to the receiver, then for \(T_s = 100\) ps and 6 bits resolution

\[
f_{jitter-p} = 8\text{ ps}
\]

If a T-tapped digital equalizer is used after the ADC, then the ADC has to sample each bit once. This means a sampling rate of 10 GSample/s is needed for the ADC. However, the highest reported 6-bit CMOS ADC sampling rate is 1.6 GSample/s [5]. This sampling rate was attained using a flash ADC in 0.18 μm CMOS technology. Therefore, the only technique that can be used to achieve a 10 GSample/s sampling rate is time-interleaving a number of high-speed ADCs. In this approach a number of ADC’s with interleaved sampling times are used as if they are a single ADC with sampling rate much higher than that of any of them. Time-interleaved architecture was first introduced in [6] and since then it has been used to time-interleaved pipelined ADC’s and flash ADC’s. The sampling rate of the formed ADC is equal to the sampling rate of individual interleaved ADC multiplied by the number of ADC’s. A PLL based clocking circuitry should provide the interleaved stages with sampling clock. To relax the sampling rate requirements on each of the interleaved ADC’s, a high number of interleaved stages would be preferred. However, the sampling clock jitter derived in (6) sets an upper bound on the number of stages that could be interleaved. Assuming a peak to peak clock jitter of 2% [7] then

\[
f_{jitter-p} = \frac{T_{interleaved-sampling}}{2\% T_{sampling}} = 2\%
\]

where \(T_{interleaved-sampling}\) is the period of interleaved ADC’s clock

The number of interleaved stages (M) is given by

\[
M = \frac{T_{interleaved-sampling}}{T_{sampling}} = \frac{f_{jitter-p}}{2\% T_{sampling}} = \frac{8\text{ ps}}{2\% \times 100\text{ ps}} = 4
\]

Therefore, four interleaved ADC’s each with a 2.5 GS/s can be used to achieve a total sampling rate of 10 GS/s and satisfy jitter requirements at the same time. Since the flash ADC is the fastest analog to digital structure [3], it is the best candidate for implementing the interleaved ADC’s for OC-192. The differential nonlinearity (DNL) of individual ADC’s should be kept below 0.5 LSB to guarantee no missing codes, while a maximum of 1 LSB is allowed for integral nonlinearity to keep the worst case effective number of bits (ENOB) > N-1 bits [8]. The derived ADC specifications required for OC-192 receiver are summarized in Table 1. The analog bandwidth of the ADC is chosen to be 7 GHz. This is 0.7 times the input data rate. This value is chosen as a compromise to keep both ISI and integrated noise low [9].

Although, time-interleaving relaxes the sampling rate requirements of individual ADC’s, the sample and hold circuit of the ADC still needs to track the full signal bandwidth. Moreover the sample and hold circuit should achieve a higher linearity than the ADC (6 bits) to give a margin for error introduced by the quantizer and interpolating. Therefore, the sample and hold circuit is required to track a 7 GHz input bandwidth at 2.5 GHz sampling rate with more than 6 bits of linearity. Comparing this performance to the state of the art [5] CMOS sample and hold reveals that the sample and hold circuit is a main bottleneck in implementing this architecture.

Fig. 3 SNR at the output of the ADC vs. ADC resolution (number of bits)

![Fig. 4 Uncertainty of sampling instant](image)

### Table 1 Derived ADC specifications

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Interleaved flash ADC's</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of interleaved stages</td>
<td>4</td>
</tr>
<tr>
<td>Number of bits</td>
<td>6</td>
</tr>
<tr>
<td>Total sampling rate</td>
<td>10 GSample/s</td>
</tr>
<tr>
<td>Analog bandwidth</td>
<td>7 GHz</td>
</tr>
<tr>
<td>DNL</td>
<td>±1 LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>±3/4 LSB</td>
</tr>
<tr>
<td>Sampling clock jitter</td>
<td>≤ 8 ps p-p</td>
</tr>
</tbody>
</table>

### III. HIGH SPEED CMOS SAMPLE AND HOLD

Sample and hold circuits can be classified into either open loop or closed loop architecture. Open loop architecture is best suited for high speed applications, while closed loop topology is used in high precision applications.

Almost all reported high speed CMOS ADC’s used a simple sample and hold circuit consisting of an NMOS switch, which samples the signal on a holding capacitance as shown in Fig 5 [10]
Although this simple circuit can achieve very high sampling rates, it is not adequate for large bandwidth application or, in other words, high input frequencies as explained in this section.

The simple pseudo-differential circuit of Fig.5 switches from track to hold at the moment the input signal plus the NMOS transistor threshold voltage equals to $V_{CLK}$. Hence, the sampling instant depends on the value of the input signal. This causes distortion to the output signal [8].

For the pseudo-differential circuit of Fig.5, even order harmonics are cancelled and it is the odd order harmonics that limits the signal to distortion ratio (SDR). The signal to distortion ratio of this circuit is limited to [8]

$$SDR = 40 \log_{10} \left( \frac{V_{clock}}{a f_{sig} T_{s}} \right)$$

where $f_{sig}$ is the input signal frequency, $T_{s}$ is the sampling clock fall time, $a$ is the input signal amplitude and $V_{clock}$ is the sampling clock amplitude. The circuit of Fig.5 is designed in 0.13μm CMOS technology and simulated on HSPICE with extracted parasitics. In this simulation four sample and hold circuits (each running at 2.5 GS/s) were interleaved together (Fig.6) and an input signal of frequency equal to 4.7656 GHz was applied to the system. A common mode voltage $0.2$V was used to lower switch resistance.

The obtained samples from sample and hold circuits were imported to MATLAB to be multiplexed into a one 10 GS/s stream. The result of a 128 point FFT of the resulting stream is given in Fig.7. The second order harmonics are cancelled due to differential operation, while the third order harmonic is folded back to 4.2969 GHz ($\approx 3 \times 4.7656$Hz-10GHz). An SDR = 40.08 dB is obtained from simulations. The value obtained from (9) for $f_{sig}$=4.7656 GHz, $T_{s}$=60 ps, $a=0.15V$ and $V_{pp}$=1.2 is 42.1 dB. Note that the value estimated by (9) is approximately equal to the value of SDR obtained from HSPICE simulations, although (9) considers distortion due to input dependent sampling instant only. This is because input dependent sampling instant distortion is function in input signal frequency hence at high frequencies it becomes the dominant source of nonlinearity.

$$SNDR = \frac{S_{f}}{D + N_{d} + N_{s} + N_{f} + N_{s} \cdot \frac{1}{1 + \frac{S_{f}/N_{d}}{S_{f}/N_{s}} + \frac{1}{S_{f}/N_{b}}}}$$

$$SNDR = \frac{1}{S_{f}/N_{d} + S_{f}/N_{s} + S_{f}/N_{b}}$$

where $D$ is the total distortion power, $N_{d}$ is the noise power due to gain mismatch, $N_{s}$ is the noise power due to offset mismatch, $N_{f}$ is the noise power due to sampling time mismatch, $\sigma_{d}$ is the RMS value of the ADC's gains, $\sigma_{s}$ is the RMS value of the ADC's offsets and $\sigma_{f}$ is the RMS value of the clock jitter. Eq. (10) is modified version than that in [6] that takes into account bit synchronization with sampling clock. Using SDR obtained from simulation and typical values for $\sigma_{d}$ (0.5%), $\sigma_{s}$ (0.1 LSB) and $\sigma_{f}$ (1.3 ps), SDR would equal to 34.5 dB (5.4 bits). Therefore, in a practical design this circuit would leave a very tight headroom for errors due to DNL and INL. Actually, the SDR of the sample and hold circuit is usually designed to be from 6 to 12 dB above the quantization noise [12]. Given that the SDR of this circuit is only 40.08dB, it can be concluded that it is not adequate for 6-bit operation.

**Fig.5 Pseudo - differential sample and hold circuit**

Unfortunately, the performance of interleaved ADC is sensitive to mismatches between different stages. The three main sources of mismatch in time interleaved structure are offset, gain, and sample time mismatches. These errors are uncorrelated and the noise power they introduce can be added. If these errors are considered then the signal to noise + distortion ratio (SNDR) is given by [6]

$$SNDR = \frac{S_{f}}{D + N_{d} + N_{s} + N_{f} + N_{s} \cdot \frac{1}{1 + \frac{S_{f}/N_{d}}{S_{f}/N_{s}} + \frac{1}{S_{f}/N_{b}}}}$$

$$SNDR = \frac{1}{S_{f}/N_{d} + S_{f}/N_{s} + S_{f}/N_{b}}$$

A typical value for the output differential signal amplitude after AGC is 0.3V. therefore “a” which is the amplitude of the single ended signal is taken $= 0.15V$.

**IV. THE PROPOSED SAMPLE AND HOLD CIRCUIT**

To eliminate distortion due to input dependent sampling the sampling signal $V_{CLK}$ must be bootstrapped such that $V_{CLK} = v_{i} + V_{pp}$ and hence $V_{GS}$ of the NMOS switch $= V_{G} - V_{S} = V_{pp} + V_{tr}$ $v_{i} = V_{pp}$. Previously, reported bootstrapped circuits [13] [14] were mainly designed for switched capacitor and low speed applications and therefore can not be used for this application because they lack either the required wide bandwidth (7 GHz) and/or can not sample at the target sampling rate of 2.5 GS/s.
The proposed sample and hold circuit is shown in Fig. 8. Only half of the circuit is shown for clarity. A level shifter $M_{p1}$ is used to shift the common mode voltage of the input signal from $V_{in}$ to $V_{DD}$. When $V_{DD}$ is high $M_s$ is OFF, $V_{i} + V_{DD}$ is passed to the gate of $M_s$, and the circuit tracks the input. In the next half cycle, $M_{s}$ turns OFF and $M_{s}$ turns ON pulling the gate of $M_{s}$ to ground and so the sample is held on the capacitor $C_{hold}$. The main reason for inserting $M_{s}$ is to isolate the level shifter keeping the DC potential at node $x$ equal to $V_{DD}$ when $M_{s}$ gate voltage falls to ground. This way the time delay that would have taken node $x$ to rise form ground to $V_{DD}$ in absence of $M_{s}$ is eliminated, allowing the circuit to work at high sampling rates. Both the boot-strapping part of the circuit and the sample and hold part are designed for a 7 GHz bandwidth so that the signal experiences the same delay when propagating through both of them. Thus, the AC signals at the gate and source of $M_{s}$ are in phase. In Fig. 8, $V_{in} = 0.2$ V, $V_{s} = 1$ V, $V_{DD} = 1.2$ V, $V_{DD} = 1.5$ V. Although $V_{DD}$ is higher than the nominal supply voltage of the technology, the drain-source voltage of $M_{s}$ is kept well below the maximum allowed drain-source voltage for transistors in this technology ($V_{DD_{max}} = 1.6V$) to avoid hot electron effects. Also, $V_{DD}$ and $V_{DD}$ are maintained at 1 V and 0.5V. This is less than the nominal technology $V_{DD}$ (1.2 V) and much less than the breakdown voltage of $t_{ox}$ for this technology ($V_{DD_{max}} = 1.6V$).

Two test setups were used for simulating the proposed circuit on HSPICE. In the first setup the circuit was operated at a sampling rate of 2.5 Gs/s with a 0.918 GHz input frequency. Fig. 9 shows that the proposed circuit leads to a 9.9 dB reduction in the third harmonic. In the second test setup, the proposed circuit was used to build the structure of Fig.6 and an input signal of 4.768 GHz was applied to its input as carried in Section III for the conventional sample and hold. The output spectrum is shown in Fig.10. Comparing Figs.6 and Fig.7, it can be concluded that the proposed circuit leads to a 13.6 dB reduction in the third order harmonic achieving an SDR = 53 dB. Using (10), the proposed sample and hold leads to effective number of bits (ENOB) = 5.7. This allows ADC built with the proposed sample and hold to achieve the required accuracy (> 5 effective bits) in the presence of other errors due to interleaving.

![Fig. 8: The proposed sample and hold circuit](image)

**V. CONCLUSIONS**

Robust digital equalizers can be used at the receivers of high-speed communications; if a 6 bit-10 GSamples/s ADC is implemented. Time-interleaved structure is the only structure that can achieve a sampling rate of 10 GS/s in CMOS. It was shown that four interleaved ADC’s each with a 2.5 GS/s can be used to achieve a total sampling rate of 10 GS/s and satisfy jitter requirements at the same time. Although, time-interleaving relays the sampling rate requirements of individual ADC’s and hence sample and hold circuits to 2.5 GS/s, the sample and hold circuits still need to track the full system bandwidth of 7GHz. Simple NMOS-switch based sample and hold circuits can sample at the target sampling rate. However, they can not be used for high input frequencies since they suffer from input dependent sampling instant distortion that is function in input signal frequency. Therefore, a boot-strapped sample and hold circuit is proposed. The proposed sample and hold achieves a SDR = 53 dB at desired input frequency and sampling rate. This gives a large margin for other sources of errors introduced by interleaving and allows ADC built with the proposed sample and hold to achieve the required resolution (6 bits) in the presence of other errors introduced by interleaving.

![Fig. 9: The output spectrum of (a) Proposed sample and hold and (b) conventional sample and hold. Input frequency is chosen = 49/128 x f_{sampl}, where f_{sampl} = 2.3 GHz](image)

![Fig. 10: Output signal spectrum from the structure of Fig.6 built with the proposed sample and hold. Input frequency is chosen = 61/128 x f_{sampl}, where f_{sampl} = 10 GHz](image)

**REFERENCES**


