Analysis and Design of Low-Power Multi-Threshold MCML

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Abstract
Multi-threshold MOS current mode logic (MTMCML) is a natural evolution for MCML that offers power saving through supply voltage reduction while retaining the same performance. In this work, analytical formulation based on the BSIM3v3 model is proposed for MTMCML with error within 10% compared to HSPICE. The formulation helps designers to efficiently design MTMCML circuits without undergoing the time-consuming HSPICE simulations. Furthermore, it provides design guidelines and aids for designers to fully understand the different tradeoffs in MTMCML design. In addition, the analysis is extended to study the impact of technology scaling and parameter variations on MTMCML. It is shown that the worst case variation in the minimum supply voltage of MTMCML is 1.16%, thus suggesting maximal power saving.

1 Introduction
With the explosion in transmission speeds of communication systems, the demand for very high-speed VLSI circuits is on the rise. Although the performance of CMOS technologies improves notably with scaling, yet conventional CMOS circuits could not satisfy all of the speed and power requirements of these applications. MOS current mode logic (MCML) has emerged as a logic style that can achieve the much needed high-speeds while consuming less power than conventional CMOS circuits at these high-frequencies [1].

In MCML circuits, a constant current $I$ generated by $M_1$ is steered through the $ON$ branch, according to the inputs. This results in reduced output voltage swings at the circuit differential outputs ($Q$ and $\bar{Q}$); $V_{DD}$ and $V_{DD} - \Delta V$ at the OFF and ON output branches, respectively (Figure 1). $\Delta V$ is the voltage drop across $R$ ($\Delta V = I \times R$).

For MCML to be a big contender for wireless system-on-chip implementations, further work is still needed to reduce their power dissipation. Power consumption $P_d$ in MCML can be decreased by either reducing the supply voltage $V_{DD}$ or the current $I$ ($P_d = I \times V_{DD}$). Decreasing $I$ will degrade the performance of MCML, while reducing $V_{DD}$ is limited by the minimum supply voltage needed for proper operation. Hence, a method to safely reduce $V_{DD}$ is needed.

Recently, multi-threshold CMOS\(^1\) (MTCMOS) started to gain attention from the analog circuit industry to achieve other goals than leakage reduction [4]. In [5], MTMCOS was used to enable further reduction in the supply voltage of MTMCML circuits, thus decreasing the total static power dissipation. MTMCML proved its effectiveness in reducing power dissipation by 20% when compared to conventional MCML [5].

Although MTMCML was introduced in [5], yet a complete analysis for all of the circuit design parameters together with design guidelines for MTMCML designers were not presented. The analysis presented in [5] for MTMCML was based on inaccurate long-channel modeling equations, which are inappropriate to use in today’s deep sub-micron technologies. In addition, the impact of technology scaling and parameter variations on MTMCML circuits has not been investigated.

In this work, a comprehensive MTMCML analytical formulation based on the BSIM3v3 model is proposed to give designers a prospective of the different tradeoffs in the design of MTMCML. To verify the accuracy of the formulation,

\(^1\)MTCMOS has been widely used to minimize leakage while retaining high performance in digital circuits by combining the fast but leaky low $V_{th}$ (LVT) devices and the less leaky but slow high $V_{th}$ (HVT) devices [2], [3].
lation, it is used in an automated methodology [6] to design several popular MTMCML benchmarks in a 0.18μm CMOS technology. The formulation is further verified by investigating MTMCML’s performance as technology scales down and under worst case parameter variations.

A closed form expression for the minimum supply voltage in MTMCML is derived in Section 2. Section 3 discusses the proposed MTMCML analysis while presenting design guidelines and tradeoffs. The analysis is verified in Section 4 by designing several MTMCML benchmarks. Finally, the impact of technology scaling and parameter variations on MTMCML are discussed in Sections 5 and 6, respectively.

2 Minimum Supply Voltage

Reducing the supply voltage in MCML will effectively decrease the power dissipation. However, the proper operation of the circuit sets a limitation on how low $V_{DD}$ can go. In a conventional 2-level MCML circuit, $M_2$ and $M_3$ are operating in the saturation and triode regions, respectively. The minimum supply voltage of MCML is given by

$$V_{\text{min}} = V_{\text{dsat},1} + V_{\text{ds},2} + V_{\text{gs},3},$$

(1)

where $V_{\text{ds}}$ and $V_{\text{dsat}}$ are the triode and saturation drain-source voltages, respectively, and $V_{\text{gs}}$ is the gate-source voltage. The supply voltage of MCML can be reduced by forcing $M_2$ into saturation ($V_{\text{dsat}} = V_{\text{ds}}$). That was achieved by using level shifters to reduce the input voltage to $M_2$. However, level shifters are power and area expensive.

MTMCML eliminates the use of level shifters by assigning LVT devices to $M_3$. On the other hand, from (1), assigning LVT devices to $M_2$ or $M_1$, results in an increase in $V_{\text{min}}$, thus they are kept as HVT devices. Figure 2 shows that $V_{\text{min}}$ decreases with decreasing $V_{\text{th},3}$ and $I$.

![Figure 2. Minimum supply voltage of MTMCML circuits.](image)

Figure 2 dictates that reducing $I$ can further allow a decrease in $V_{\text{min}}$. Thus, MTMCML circuits operating at lower speeds (for the same $\Delta V$ circuits operating at lower speeds require smaller $I$) can offer more supply voltage reduction and hence, power saving, than circuits operating at higher speeds.

3 Analytical Formulation of MTMCML Design Parameters

The design parameters of MTMCML are: delay $t_d$, voltage gain $A_v$, noise margin $N_M$, and voltage swing ratio $V_S$. In order to give accurate design guidelines for MTMCML, BSIM3v3 model [7] is used in the analytical formulations.

3.1 Circuit Delay ($t_d$)

For a 2-level MCML circuit, $t_d$ is approximated by

$$t_d = 0.69RC,$$

(5)

where $R$ is the load resistance and $C$ is the total load capacitance consisting of $C_L$ and the parasitic capacitance of $M_2$. From (5) it is noticed that by keeping the size of $M_3$ and $R$ fixed, MTMCML and conventional MCML will have equal $t_d$.

3.2 DC Voltage Gain ($A_v$)

$A_v$ is defined as the mid-swing DC voltage gain. For a 2-level MCML circuit, $A_v$ is expressed as

$$|A_v| = \frac{Rg_m}{g_{m2} + g_{m3}},$$

(6)

where $g_m$ is the MOS transconductance. In MTMCML, both $M_2$ and $M_3$ are operating in saturation, hence, $A_v$ is given by

$$|A_v| = \frac{2\mu_mC_ oxI}{\sqrt{2\mu_mC_ ox I^2 + 2\mu_mC_ oxW_2L_2} + \sqrt{W_2L_2I}}.$$
By inspecting (6), it is observed that $A_u$ for MTMCML is smaller than that in MCML for the same transistor sizes and current values. This is explained by the fact that $g_m$ in saturation is less than that in the triode region. Figure 3 plots $A_u$ in MTMCML against $W_3$ for different $W_2$ values as well as the conventional MCML case. Figure 3 shows that $A_u$ for MTMCML is less than that in conventional MCML by about 30%. To avoid degrading MTMCML's performance and achieve similar $A_u$ values as MCML, $W_2$ is sized up.

![Figure 3. $A_u$ for MTMCML and MCML circuits.](image)

$A_u$ is responsible for giving the MTMCML circuit regeneration and stability and is usually designed to be larger than unity. On the other hand, increasing $A_u$ degrades $t_d$. Practically, a small margin (40%) above the unity gain is needed, accordingly, in this work a minimum $A_u$ of 1.4 is used [8].

### 3.3 Noise Margin (NM)

NM of a 2-level MCML circuit is given by [6]

$$NM = \frac{V_{in} - \Delta V}{\sqrt{2(3\beta R)^2(R - A_u R_2)}}$$

$$\left(\sqrt{\frac{4A_u^2 R_2^2}{R - A_u R_2}} - \sqrt{(R - A_u R_2)^2 + 8A_u^2 R_2^2} + R - A_u R_2\right)$$

where $V_{in} = \sqrt{\frac{4(3R)^2}{2(R)}}(\sqrt{1 + 8(3R)^2} - 1) + \frac{V_D}{2}$, $\beta = \mu C_w W_3/L_3$, and $R_2 = 1/g_{m2}$. The dependence of $NM$ on $A_u$ is clear from (8), hence, $NM$ for MTMCML will differ from its MCML counterpart in a similar manner to $A_u$. MTMCML circuits have high noise immunity because of their differential structure, hence a small $NM$ is sufficient for proper operation. Moreover, increasing $NM$ reduces $t_d$. To best balance the two effects, $NM$ is set to 0.4 $\Delta V$ [9].

### 3.4 Voltage Swing Ratio (VSR)

VSR is the ratio of the current in the ON branch $I_{on}$ to the total current $I$. In a 2-level MTMCML, one can define VSR3 and VSR2 in the $M_3$ and $M_2$ levels of the circuit, respectively. The total circuit VSR is the product of these 2 terms. Ideally, VSR is unity (all of $I$ flows through the ON branch), but due to non-idealities in the devices, it drops below 1. Using the BSIM3v3 saturation current equations for $M_3$ and $M_2$, VSR3 and VSR2 are given by

$$VSR_3 = \frac{V_{DD} - V_{th,3}}{2(V_{DD} - V_{th,3} - V_{sat,3ff} - V_{sat,3on} - \Delta V)}$$

$$VSR_2 = \frac{V_{DD} - V_{th,2}}{2(V_{DD} - V_{th,2} - V_{sat,2ff} - V_{sat,2on} - \Delta V)}$$

where $V_{sat,3on}$ and $V_{sat,3ff}$ are the saturation drain-source voltages for $M_3$ in the ON and OFF branches, respectively. From (9), one can notice that the assigning LVT devices to $M_3$ will reduce VSR3, while VSR2 is independent of $V_{th,3}$. Meanwhile, if $V_{DD}$ is scaled down with $V_{th,3}$ according to (4), VSR3 will remain constant with $V_{th,3}$, as shown in Figure 4.

![Figure 4. VSR in MTMCML circuits.](image)

To provide MTMCML circuits with sufficient current switching capabilities, VSR is set to a minimum of 95%. Hence, VSR3 and VSR2 are set to a minimum of 98% [8].

### 4 Design of MTMCML Circuits

The design of MTMCML circuits is a complex problem because (1) MTMCML’s performance is a function of numerous design parameters, and (2) the proper operation of the circuit is heavily dependent on many design variables. In this work, the optimization-based design methodology presented in [6] is used to design MTMCML circuits to satisfy the design constraints given in Section 3, while minimizing power dissipation. The optimization problem is modified to account for the differences between MCML and MTMCML. Figure 5 lists the MTMCML optimization problem. All of the parameters in Figure 5 are evaluated using the formulations given in Section 3. The aim of using the optimization problem is to verify the accuracy of the proposed MTMCML formulation. $L_2$ and $L_3$ are set to the minimum feature size since they do not impact any of the design parameters mentioned in Section 3, and increasing them will increase $t_d$. $L_2$ is determined by the required output resistance of $M_1$ that results in common-mode rejection ratio (CMRR) above 20 [10].
Given: 
Required delay $t_{\text{required}}$
Minimum: 
Power dissipation $P_d$

Subject to
(i) $NM \geq 0.4\Delta V$
(ii) $\Delta V \leq V_{DD} - V_{th}$
(iii) $V_{DD} = 1 \times R$
(iv) $V_{DD} = V_{th} - \Delta V \leq V_{S} \leq V_{DD} - V_{th}$
(v) $V_{S} \geq V_{th} \geq V_{S_{\text{min}}}$
(vi) $t_d \geq t_{\text{required}}$
(vii) $V_{S} \geq V_{min}$
(viii) $CMRR \geq 10$
(ix) $I_{S} \geq 1.4$
(x) $I = W_{1} I_{in} C_{ox}(V_{S} - V_{th} - V_{S_{\text{stat}}} - V_{th})$
(xii) $V_{S} \geq 0.08$

Figure 5. MTMCMCL design optimization problem definition [6].

4.1 Benchmarks

Using the expressions in Section 3 and the optimization problem in Figure 5, several MTMCMCL benchmarks are designed in a 0.18μm CMOS technology to operate at 3GHz. The circuits designed are: -2 frequency divider, 1:16 demultiplexer, 16:1 multiplexer, 2-input AND/NAND, 2-input XOR/XNOR, and 4-bit carry-lookahead adder (CLA). The output designs from the optimization problem are listed in Table 1. The data reported for the MUX and DEMUX are for the last and first stages, respectively. Table 1 verifies that the accuracy of the formulation is less than 10% and 8% in $P_d$ and $t_d$, respectively, when compared to HSPICE. Moreover, the average power saving in the reduced $V_{DD}$ MTMCMCL ($V_{min}$ can be as low as 1.1V) is 21% compared to conventional MCML operating at their minimum supply voltage of 1.5V (Table 1).

5 Prospects of MTMCMCL as Technology Scales

With the continuous down scaling of CMOS feature size, the performance of VLSI circuits is expected to improve. In this section the impact of technology scaling on MTMCMCL is investigated using current (180nm, 130nm) and predictive (100nm, 70nm, 65nm, 45nm) [11] CMOS technologies. Figure 6 plots the scaling trends of $V_{min}$, $A_v$, $NM$, and $VSR$.

Figure 6(a) shows that the reduction in $V_{th}$ with technology scaling will allow designers to further reduce the supply voltage to achieve more power saving while attaining the required performance, with a $V_{min}$ of 0.4V expected in a 45nm CMOS technology. The reduction in $t_{oz}$ with the technology is expected to give future MTMCMCL circuits higher $A_v$, Figure 6(b). On the other hand, $NM$ saturates at about 0.63$\Delta V$, as shown in Figure 6(c). This is not a limiting factor for future MTMCMCL circuits because this is a large value when compared to $NM$ of today's MCML circuits (0.4$\Delta V$) [9]. $VSR$ also shows a saturation at a value of 0.99, which is very close to its absolute maximum of 1, Figure 6(d). The increase in $VSR$ is enabled by the reduction of $V_{th}$ with the technology. In conclusion, MTMCMCL performance is expected to improve with technology scaling while continuing to provide designers with notable power saving.

6 Impact of Parameter Variations on MTMCMCL Performance

As technology scaling continues to decrease the devices minimum feature size, parameter variations are expected to impose a growing threat on VLSI circuits functionality. Hence, designers must consider variations during the design phase, otherwise, risk malfunction and poor performance of circuits. Sources of parameter variations include environmental variations ($V_{DD}$, temperature $T$) and process variations (transistors length $L$, oxide thickness $t_{ox}$, doping profile $N_{A}$, threshold voltage $V_{th}$, mobility $\mu$, interconnect width $w$).

Since MTMCMCL circuits have an analog operational behavior, parameter variations can notably affect their functionality like all analog circuits. As a way to design MTMCMCL circuits for variability, the design dependence for worst case variations (3σ point) of all the circuit parameters affected by parameter variations is modeled. Using the optimization problem in Figure 5 while accounting for worst case parameter variations, the benchmarks designed in Section 4.1 are redesign for worst case variations. Table 2 lists the changes needed in each of the circuit parameters to account for variations. Table 3 lists the equations used in modeling the impact of parameter variations on $t_d$, while the impact of variations on the other design parameters is not listed for space constraints.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>$W_1$ (μm)</th>
<th>$W_2$ (μm)</th>
<th>$R$ (kΩ)</th>
<th>$\Delta V$ (mV)</th>
<th>$V_{S}$ (V)</th>
<th>$V_{th}$ (V)</th>
<th>$L_{c}$ (μm)</th>
<th>$P_{\text{model}}$ (μW)</th>
<th>$P_{\text{HSPICE}}$ (μW)</th>
<th>% error in $P$</th>
<th>$V_{DD}$ (V)</th>
<th>% $P_d$ Saving</th>
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<tbody>
<tr>
<td>Freq divider</td>
<td>4.8</td>
<td>8.84</td>
<td>4.02</td>
<td>200</td>
<td>0.684</td>
<td>2.64</td>
<td>1.74</td>
<td>136.72</td>
<td>147.6</td>
<td>8.43</td>
<td>1.16</td>
<td>22.46</td>
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<tr>
<td>1:16 Demux</td>
<td>5.76</td>
<td>6.68</td>
<td>6.82</td>
<td>200</td>
<td>0.78</td>
<td>1.94</td>
<td>1.06</td>
<td>337.5</td>
<td>359.7</td>
<td>6.17</td>
<td>1.22</td>
<td>18.71</td>
</tr>
<tr>
<td>16:1 Mux</td>
<td>3.74</td>
<td>9.72</td>
<td>4.56</td>
<td>200</td>
<td>0.87</td>
<td>1.54</td>
<td>1.81</td>
<td>412.4</td>
<td>446.5</td>
<td>8.19</td>
<td>1.19</td>
<td>30.61</td>
</tr>
<tr>
<td>AND/NAND</td>
<td>1.28</td>
<td>8.62</td>
<td>5.99</td>
<td>200</td>
<td>0.87</td>
<td>1.82</td>
<td>1.98</td>
<td>434.5</td>
<td>482.2</td>
<td>8.7</td>
<td>1.67</td>
<td>31.54</td>
</tr>
<tr>
<td>XOR/XNOR</td>
<td>1.38</td>
<td>7.05</td>
<td>4.12</td>
<td>200</td>
<td>0.77</td>
<td>3.52</td>
<td>1.75</td>
<td>41.1</td>
<td>45.1</td>
<td>8.26</td>
<td>1.21</td>
<td>19.92</td>
</tr>
</tbody>
</table>

Table 1. Design of high performance MTMCMCL circuits operating at 3GHz.
the impact of parameter variations on its value. To find out the amount of guard band needed for $V_{\text{min}}$, the dependence of $V_{\text{min}}$ on variations in its parameters is modeled. The percentage variation in $V_{\text{min}}$ due to the change in each and all (worst and best cases) of its parameters are listed in Table 4. From Table 4, it can be concluded that parameter variations will have minimal impact on $V_{\text{min}}$ (only 1.16% variation). Hence, MTMCML designers can fully benefit from the reduced supply voltage with a small guard band to account for variations.

Table 4. Impact of parameter variations on $V_{\text{min}}$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>% Variation</th>
<th>% Variation in $V_{\text{min}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L$</td>
<td>-10%</td>
<td>-0.53%</td>
</tr>
<tr>
<td>$t_{oa}$</td>
<td>10%</td>
<td>0.48%</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>-10%</td>
<td>-1.21%</td>
</tr>
<tr>
<td>$N_{OA}$</td>
<td>10%</td>
<td>1.15%</td>
</tr>
<tr>
<td></td>
<td>-10%</td>
<td>-0.3%</td>
</tr>
<tr>
<td></td>
<td>10%</td>
<td>0.3%</td>
</tr>
<tr>
<td>Best Case</td>
<td>-1.21%</td>
<td>1.16%</td>
</tr>
</tbody>
</table>

7 Conclusion

In this work, a comprehensive analytical formulation for MTMCML based on BSIM3v3 is proposed with a maximum error of 10% when compared to HSPICE. Moreover, it was shown that MTMCML designers will lose only a small part of the power saving (1.16%) for guard banding against variations. Studying the impact of technology scaling on MTMCML showed that MTMCML supply voltage will continue on decreasing to provide notable power saving with a minimum supply voltage of 0.4V expected at a 45nm CMOS process.

References