

**IEEE Kitchener-Waterloo**

**"Minimum Transmit Redundancy FIR  
Precoder-Equalizer System Design"**

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**Time: 10:00 am**

**Location: MC 5158**

This seminar is a part of a series of invited talks (Distinguished Seminar Series, <http://www.dss.uwaterloo.ca>) and is co-sponsored by the coding and Signal Transmission Laboratory, E&CE Dept., Univ. of Waterloo, <http://www.cst.uwaterloo.ca>, Communications and Information Technology Ontario (CITO), <http://www.cito.ca>, IEEE Information Theory Society, Kitchener-Waterloo Chapter, [http://www.ece.uwaterloo.ca/~ieeee\\_kw/](http://www.ece.uwaterloo.ca/~ieeee_kw/), Institute for computer Research (ICR), <http://www.icr.uwaterloo.ca>, and Nortel Networks Institute for Advanced Information Technology at the University of Waterloo, <http://www.nortel-institute.uwaterloo.ca>. For further information, please contact: [khandani@cst.uwaterloo.ca](mailto:khandani@cst.uwaterloo.ca)

**All Are Welcome!**

**Abstract**

The communication problem caused by selective fading channel can be alleviated by precoding the signal to be transmitted. The precoder adds redundancy to the transmitted signal that can be exploited by zero-forcing equalizer. However, the inserted redundant signal consumes channel bandwidth, which affects the system throughput. In this talk we will discuss ways to reduce the amount of inserted redundancy to maximize system throughput. The minimum amount of redundancy and the corresponding requirements for the existence of FIR zero-forcing precoder-equalizer system are characterized. A systematic design method is proposed together with various design criteria for the precoder-equalizer system will be discussed under the non-maximally decimated filter banks framework. Extension to MIMO communication systems will also be discussed. Finally, a jointly optimized precoder-equalizer design method, a FIR zero-forcing equalizer with successive interference cancellation, and other precoder-equalizer optimization are presented together with simulation results that show significant improvement in lowering the bit error rate can be obtained.

**Biography**

Chi-Wah Kok received the B.Eng and MPhil degrees from the City University of Hong Kong in Electronic Engineering in 1990 and 1993 respectively. After working in several semiconductor companies which include Lattice Semiconductor, in 1993 to 1995, he joined the University of Wisconsin, Madison in 1995, and earned the MSc and PhD degrees in Electrical Engineering in 1996 and 1997 respectively. Upon graduation, he joined the SONY US Research Laboratory and Stanford University. Since 1999, he has been with the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology as an assistant professor. He has published more than 100 archival papers in the area of signal processing with applications in multimedia and digital communications.