IEEE KITCHENER-WATERLOO

IEEE MTT-Chapter Presentation

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"Power-Aware Branch Prediction"

Abstract:
The goal of the work presented in this talk is to reduce branch predictor energy consumption without harming accuracy and hence overall performance. Reducing branch predictor's energy consumption is important for two reasons: First, branch predictors already account for a large fraction of on-chip dynamic power dissipation. Second, their power is bound to increase as further improvements in prediction accuracy may call for even larger and more complex branch predictors. The trivial option of reducing energy by using smaller predictors is not acceptable as that would lead to unacceptable accuracy and hence performance degradation. In fact maintaining and if possible improving prediction accuracy is necessary since it is essential for future processors that will be required to look further in the instruction stream in order to tolerate slower main memories and deeper pipelines.
In this talk we introduce power efficient techniques that exploit instruction behavior to reduce predictor energy. We use branch instruction past behavior to eliminate unnecessary predictor accesses. We show that it is possible to save branch predictor energy consumption while maintaining performance by:

1.. Eliminating unnecessary sub-predictor lookups, as branch instructions tend to access the same sub-predictor repeatedly.

2.. Eliminating unnecessary predictor updates for well-behaved branch instructions, which there is already enough information available to the predictor to predict their outcome accurately.

Key to success of our heuristics is power-efficient techniques that could identify well-behaved branches accurately and without compromising performance. We suggest techniques that do so by taking into account branch confidence and temporal locality.

Biography:
Amirali Baniasadi received his BS degree in electronics and electrical engineering from Tehran University, Tehran, Iran, in 1993. He received his MS degree in digital electronics from Sharif University of Technology, Tehran, Iran in 1995. He received his PhD degree in computer engineering from Northwestern University, Evanston, IL, USA in 2002. He is currently an assistant professor at the ECE department of University of Victoria, Victoria, BC. His current research interests include low-power microarchitecture, complexity-effective design and clustered processors.

DATE: **Monday May 3, 2004**

TIME: **3:00-4:30 pm**

LOCATION: EIT 3142, University of Waterloo

Invited by Professor Mohab Anis
Electrical & Computer Engineering Department