IEEE KITCHENER-WATERLOO
EDS/SSC Chapter Presentation

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NanoImprint Lithography (NIL) Enabling Nano-Technology

Abstract:
The semiconductor Industry is driven by the pursuit of maintaining "Moore's Law", the exponential growth of the number of transistors packed onto a microchip, obtained by the ability of lithographers to pattern ever smaller and smaller dimensions. With the limitations of traditional photolithography becoming more apparent, a variety of new lithographies are being developed as possible next generation candidates.

NanoImprint Lithography (NIL), a technology developed in the NanoStructure Laboratory by Professor Stephen Y. Chou, is one such candidate. NIL stands alone in achieving feature fabrication as small as 5 nm and 12 nm pitch, while capable of patterning an entire wafer simultaneously, with extraordinarily low cost. This performance has not only attracted the interest of the semiconductor industry, but researchers and corporations world-wide who wish to explore the exciting and rapidly growing field of nano-technology.

In this talk, Michael Austin will discuss NIL's performance and some of the nano-applications developed in the NanoStructure Laboratory to take advantage of NIL's unique capabilities.

DATE: **Friday, October 1, 2004**

TIME: **4:00 pm**

LOCATION: **EIT 3142, University of Waterloo**

Invited by Prof. A. Nathan
Electrical & Computer Engineering IEEE Presentation
All are Welcome! Refreshments Available