



IEEE KW Section



IEEE Solid-State Circuit Chapter Presentation

A Road-Map to Clock and Data Recovery Circuit Design for SERDES Applications

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Abstract: This talk presents functional characteristics and design challenges associated with a serializer-deserializer (SERDES) system, as well as economical background for the fast growing SERDES industry. An approach to design clock and data recovery circuits (CRC's), that are the core base of a SERDES system is included, providing a brief summary of the design and the necessary verifications of a CDR building blocks. This talk also includes a brief summary of a 9-16 Gb/s clock and data recovery circuit that has been designed, and successfully tested in a standard CMOS 0.18um technology.

Afshin Rezayee received the B.A.Sc. and M.A.Sc. degrees from Isfahan University of Technology, Isfahan, Iran in 1995 and 1997, respectively. He was awarded the Ph.D. degree from the University of Toronto, Toronto, Ontario, Canada in 2003. He worked at the Electrical and Computer Engineering Research Centre of Isfahan University of Technology from 1997-1999, where he was involved in developing an AFE for wireless applications. He joined Snowbush Microelectronics, Toronto, Ontario, Canada in 2002 and has been engaged in the research and development of mixed-mode CMOS circuits. His topics of interest are clock and data recovery circuits, frequency synthesizers, analog front-ends, data converters and switching regulators. Afshin Rezayee won the best student paper award at MWSCAS 2001, Dayton, Ohio, USA in 2001. He received the Edward S. Rogers Scholarship in 2001. He and his colleagues in Electrical and Computer Engineering Research Centre of Isfahan University of Technology won the silver price of "Kharazmi" research competitions, Tehran, Iran, in 1999.

Invited by S. Ardalan