IEEE KW Section

IEEE Solid-State Circuit Chapter Presentation

1. The Use of Feedback in Common Gate LNAs for Multi-standard Terminals

2. Single-Stage Low Power Quadrature RF Receiver Front-End: The LMV Cell

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Abstract:

The use of feedback in common gate LNAs for Multistandard terminals (30 min.)
This presentation is focused on new topologies of low noise amplifier (LNA) aimed towards multistandard applications. For its position at the beginning of the RX chain, the multistandard LNA can provide a reconfigurable frequency selection of the standard received or a concurrent reception over a wide bandwidth. While common source/emitter structures has been deeply studied in the past years, reaching the state of art with the inductively degenerated topology, the common gate/base configuration has been often neglected due to the high noise produced under matching condition. In this presentation it will be shown as the introduction of several kind of feedback around the common gate/base configuration can reduce the amplifier noise figure and adds multistandard capabilities such as wideband input matching or reconfigurability.

Single-Stage Low Power Quadrature RF Receiver Front-End: The LMV cell (15 min.)
This second brief lecture presents the first quadrature RF receiver front-end where in a single stage, low noise amplifier (LNA), mixer and voltage controlled oscillator (VCO) share the same bias current. The new structure exploits the intrinsic mixing functionality of a classical LC-tank oscillator providing a compact and low power solution, compatible with low voltage technologies. A 0.13mm CMOS prototype tailored to the GPS application is presented. The experimental results exhibit a noise figure of 4.8dB, a gain of 36dB, an IIP3 of -19dBm with a total power consumption of only 5.4mW from a voltage supply of 1.2V.

Antonio Liscidini was born in Tirano, Italy, in 1977. He received the Laurea degree (*summa cum laudae*) and PhD. in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006 respectively. He was a summer intern at National Semiconductors in 2003 (Santa Clara, CA) studying poly phase filters and CMOS LNA. Currently he has a post-doc position at University of Pavia and his research interests are in the implementations of analog RF front-end in CMOS and BiCMOS technology, with particular focus on the analysis and design of LNAs for multistandard applications, ultra low power receivers and digital PLLs. In addition to his academic activities, he has been acting as a consultant for Marvell Semiconductors in the area of integrated circuit design. He received the Best Student Paper Award at IEEE 2005 Symposium on VLSI Circuits