HourGlass: Predictable Time-based Cache Coherence Protocol for Dual-Critical Multi-Core Systems

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Abstract—We present a hardware mechanism called HourGlass to predictably share data in a multi-core system where cores are explicitly designated as critical or non-critical. HourGlass is a time-based cache coherence protocol for dual-critical multi-core systems that ensures worst-case latency (WCL) bounds for memory requests originating from critical cores. Although HourGlass does not provide either WCL or bandwidth guarantees for memory requests from non-critical cores, it promotes the use of timers to improve its bandwidth utilization while still maintaining WCL bounds for critical cores. This encourages a trade-off between the WCL bounds for critical cores, and the improved memory bandwidth for non-critical cores via timer configurations. We evaluate HourGlass using gem5, and with multi-threaded benchmark suites including SPLASH-2, and synthetic workloads. Our results show that the WCL for critical cores with HourGlass is always within the analytical WCL bounds, and provides a tighter WCL bound on critical cores compared to the state-of-the-art real-time cache coherence protocol. Further, we show that HourGlass enables a trade-off between provable WCL bounds for critical cores, and improved bandwidth utilization for non-critical cores. The average-case performance of HourGlass is comparable to the state-of-the-art real-time cache coherence protocol, and suffers a slowdown of $1.43 \times$ and $1.46 \times$ compared to the conventional MSI and MESI protocols.

I. INTRODUCTION

Modern mixed-criticality systems (MCS) consist of a combination of critical and non-critical tasks that share the hardware resources when deployed on a computing platform. For certification, it is imperative to guarantee that critical tasks never exceed their requirements. Otherwise, the system may result in catastrophic consequences. Example domains include avionics and automotive (DO 178C and ISO 26262). Non-critical tasks, however, do not require such stringent guarantees, but instead, may only require best-effort service such as improved average-case performance. A primary concern in MCS is the resulting interference caused by the critical and non-critical tasks sharing the hardware resources. This is because the non-critical tasks can contribute to the worst-case execution time (WCET) of the critical tasks or it may significantly complicate the WCET analysis. The contributing interference may originate from one or many of the hardware components such as the main memory, last-level caches, and shared buses. Consequently, there is considerable interest in devising strategies to mitigate the impact of such interference.

As demands for more functionality from MCS increase, there is noticeable interest in leveraging multi-core platforms to deploy such applications (Freescale P4080, [1]). While using multi-cores reduces hardware cost, it also offers parallelism that applications can exploit. However, they also introduce additional sources of interference. One such interference occurs when multiple tasks deployed on different cores access shared data that is temporarily stored in the private cache of a core. Since multiple threads may update the shared data, ensuring that any read of the shared data receives the most up-to-date write to the shared data is essential for correct execution. This involves transferring the data from one private cache, through the bus, to the requesting core’s cache. Since the worst-case latency (WCL) to access data is a component of the WCET, predictably managing transfers of shared data between critical and non-critical tasks remains a challenging problem [2].

Recently, a hardware-based cache coherence protocol to predictably manage accesses to shared data in multi-cores called PMSI [3] was proposed. However, PMSI assumed only critical tasks, and a non-critical task would be treated as a critical task. As a result, a non-critical task would cost the critical tasks an opportunity for tighter worst-case latency bounds. Furthermore, PMSI does not offer any mechanisms to encourage non-critical tasks to improve its average-case memory bandwidth utilization.

In this work, we propose HourGlass, a predictable cache coherence protocol that is criticality-aware. Specifically, we design HourGlass to be a dual-critical multi-core system (DCMS) that operates on only two criticality levels: critical (cr) and non-critical (ncr). For tasks on the critical cores, we ensure worst-case latency bounds. For tasks on the non-critical cores, we provide no guarantees. However, we equip HourGlass with a timer-based mechanism to allow for tasks on non-critical cores to improve their memory bandwidth utilization. The timers allow for a trade-off between potentially improving memory bandwidth utilization of non-critical tasks while loosening the WCL bounds of critical tasks. This is acceptable if the critical tasks continue to meet their temporal requirements. HourGlass also allows for predictable sharing of data between critical tasks, and between non-critical and critical. We provide a timing analysis of HourGlass, and describe the various latency components that contribute to the WCL of requests from critical tasks. We prototype HourGlass in gem5 [4], a cycle accurate micro-architectural simulator,
and evaluate with multi-threaded benchmarks from SPLASH-2 [5], and synthetic benchmarks that exhibit maximum data sharing. We observe that the WCL of all memory requests from critical tasks are within their analytical bounds, and that timers do encourage a trade-off between bandwidth utilization of requests from non-critical cores and WCL for critical ones.

II. RELATED WORK

Multi-core real-time platforms contain interconnects, caches, and main-memory that are shared by the cores in the platform. These components are common sources of interference when multiple cores make accesses to the shared memory resulting in non-trivial timing analysis of shared data accesses. Authors in [6], [7] propose disabling shared data in the private cache hierarchies to provide timing analysis for memory requests to shared data at the cost of long execution times. Alternatively, solutions proposed in [8], [9], [10] make operating system (OS) changes to include data-sharing aware scheduler policies that identify tasks that share data, and avoid running these tasks concurrently. However, these solutions require changes to the OS, and hardware support from performance counters in order to identify tasks that share data. Another approach proposed in [11] modified the application such that accesses to shared data were protected using lock mechanisms such that the shared data was accessed by only one core at any time instance. This solution was a software implementation of cache coherence. In the worst-case, this approach performs as well as sequential execution of tasks sharing data.

A recent solution by Hassan et al. [3] proposed a hardware cache coherence protocol called PMSI to manage shared data accesses. PMSI required hardware modifications, but no changes to the OS and application. Compared to prior approaches, PMSI allowed tasks to simultaneously access copies of shared data cached in their private caches resulting in improved average-case execution time. However, PMSI was not designed for mixed-criticality systems. We believe that supporting criticality awareness in the cache coherence protocol is essential for modern real-time systems [2]. In this work, we present HourGlass, a cache coherence protocol that is criticality-aware with support for two criticality levels, which offers tighter worst-case latencies for critical cores.

There are several research efforts that provide explicit support for different criticalities in bus arbiters [12], [13], [14], [15]. Paolieri et al. [12] presented a dual-criticality arbitration where hard real-time cores (HRT) used round-robin arbitration, and whenever there were no requests from HRT, non-critical cores are serviced yielding a worst-case bound for HRT. Hassan et al. [13] presented CARb, a statically scheduled two-level bus arbitration scheme that used harmonic weighted round-robin (HWRR) arbitration. The first level performed HWRR amongst criticality classes, and the second between tasks within a criticality class. Cilku et al. [14], [15] proposed a two-layer arbiter that distinguished between memory requests from critical and non-critical cores. Their approach used TDM arbitration such that critical cores were pre-assigned slots in the TDM schedule after which a fixed number of slots were reserved to service requests from non-critical cores. Within the slots reserved for non-critical cores, round-robin was performed. HourGlass takes inspiration from Paolieri et al. [12], and Cilku et al. [14], [15], but we require no pre-allocated slots for ncr cores, which offers further opportunities for tighter worst-case latency bounds for the critical cores.

III. BACKGROUND

A. Cache coherence

Multi-core systems share data between cores by accessing addresses within a shared address space. Modern multi-core platforms implement private cache hierarchies that exploit spatial and temporal locality to improve the application’s performance. Hence, shared or private data may reside in the private cache hierarchy of multiple cores. This allows multiple copies of the data to exist in the private cache hierarchies of different cores. For correct execution of parallel programs with shared data, it is essential that any core performing a read operation on the shared data obtains the most recent write to the shared data. Since multiple copies of the shared data are privately cached across multiple cores, there must be a mechanism to ensure that reads to the shared data receive the most up-to-date data. This is known as keeping data values coherent across multiple cores.

A mechanism known as cache coherence is a solution that keeps shared data values coherent across multiple cores [16]. There are software and hardware techniques to implement cache coherence. Software approaches for cache coherence require application changes to manage the various copies of shared data explicitly. On the other hand, a hardware implementation of cache coherence implements a protocol that enforces strict rules governing the coherent view of multiple cached copies of data across multiple cores. A hardware cache controller implements this protocol. Hardware cache coherence works at the granularity of cache lines, which is the unit of data transfer in the memory hierarchy. Based on the implementation, hardware cache coherence can be realized using a snoopy shared bus, which allows all cores to observe memory activity of other cores, or using a centralized directory that co-ordinates the coherence across multiple cores [16].

In this work, we focus on hardware cache coherence that use a snoopy shared bus implementation, which we find is appropriate for current multi-core platforms with eight cores or less (Freescale P4080, [1]) used in real-time multi-core systems.

B. Coherence protocol

A cache coherence protocol is an implementation of a set of rules that ensure data coherence. This set of rules identifies states that denote the read and write permissions of cache lines, and transitions between these states that occur due to activities of other cores in the system on the same cache line. The Modified-Shared-Invalid (MSI) cache coherence protocol is a fundamental cache coherence protocol that several modern cache coherence protocols are based upon such as the MESIF,
and MOESI protocols [16]. MSI consists of three stable states. The semantics for each of these states is as follows: 1) Invalid (I) indicates that the cache line does not have valid data. 2) Modified (M) represents that the core has modified the cache line data; hence, it has the most up-to-date data. Only one core can have a cache line in the modified state. 3) Shared (S) identifies that the cache line was read, but not modified. Multiple cores may have the same cache line in the shared state. This allows read hits in their respective private caches. Cache coherence protocol also consists of transient states, which are intermediate states between stable states. These states represent whether the core is waiting for a data response, or waiting for the memory requests to be ordered on the shared bus. For example, the transient state IM^D is an intermediate state between the invalid (I) state and modified (M) state. It denotes that a core observed its write request to a cache line on the bus, and awaits a data response. A cache line changes states based on the activities of other cores. Transitions between states occur by exchanging coherence messages between the cores and shared memory.

When discussing coherence activities, we refer to the private core to identify the core whose cache controller is under consideration, and remote cores as all other cores. Since every private cache implements the same set of rules in its cache controller, we distinguish requests made by the private core and those by the remote cores. To accomplish this, a core views coherence messages on the bus as either Own or Other coherence messages. Own denotes that the cache controller observes a coherence message generated by its private core, and Other as a coherence message generated by remote cores.

IV. System Model

We assume a cache-coherent multi-core real-time system with N in-order cores \{c_0, c_1, ..., c_{N-1}\}. Each core has its own private instruction cache (L1-I) and data cache (L1-D). A core can only have one pending request to the bus. The shared memory is assumed to be the main memory. The cores and the shared memory are interconnected with a snooping bus, which exchanges coherence messages between them. Additionally, there is a common cache data bus connecting the cores to support cache-to-cache transfers. We assume that once a data transfer over the bus starts, it cannot be preempted. We characterize each core by its criticality level (cl) and the core identifier, \(c_{i}^{cl}\) where \(cl \in \{cr, ncr\}\) and \(i\) indicates the core identifier. Memory request from cr cores must have WCL guarantees per request whereas memory requests from ncr cores have no guarantees. However, ncr can benefit from improved memory bandwidth. We require that a single task is mapped to a single core for the duration of the application’s execution. However, the tasks distributed across the multiple cores can share data. We denote the number of cr cores as \(N_{cr}\), and ncr cores as \(N_{ncr}\), such that \(N = N_{cr} + N_{ncr}\). Note that we use the term cr or ncr cores interchangeably with memory requests from cr or ncr cores.

Timers improve bandwidth utilization of ncr cores. Hence, each core contains timers that enable holding onto the cache line for a fixed time duration (cycles) even when it is requested by a remote core. Once the timers expire, the private core responds to the coherence messages from the requesting remote cores. We associate two timers with each cache line for a core. The countdown timers are denoted as \(t_n(c_{n}^{cr}, c_{m}^{ncr})\) where \(t_n\) identifies the current value of the timers for \(c_{n}\), where \(n, m \in \{0, 1, ..., N - 1\}\). \(c_{n}\) denotes the core that has a valid copy of the shared data, and \(c_{m}\) denotes the requesting core. For example, assume that \(c_{i}\) is a cr core, and \(c_{j}\) is a ncr core. Then, \(t_i(c_{i}^{cr}, c_{j}^{ncr})\) denotes the timer configuration for \(c_{i}\) when a cr core \(c_{i}^{cr}\) has a valid cache line, and observes a memory request from a ncr core \(c_{j}^{ncr}\). The timers are initialized with timeout values on receiving a valid copy of the cache line. We denote \(v(cr, cr)\) as the initial timeout value for a cache line present in the private cache of a cr core, and requested by another cr core, and \(v(cr, ncr)\) as the initial timeout value for a cache line present in the private cache of a cr core, and requested by a ncr core. Similarly, we have \(v(ncr, cr)\) and \(v(ncr, ncr)\) for cache lines present in the private cache of a ncr core, and requested by another cr core and ncr core, respectively. The timeout values are precomputed based on the properties of the DCMS. Since we assume two criticality levels, a valid cache line in a cr core \(c_{i}^{cr}\) may receive requests for the cache line from a core of either of the criticality levels resulting in two timer configurations \(t_i(c_{i}^{cr}, c_{j}^{cr})\), and \(t_i(c_{i}^{cr}, c_{k}^{ncr})\) where \(c_{k}\) is another ncr core. Notice that these two timer configurations identify the requesting core to be either cr and ncr respectively. Similarly, a request to a valid cache line in a ncr core \(c_{j}^{ncr}\) also has two timer configurations \(t_j(c_{j}^{ncr}, c_{l}^{cr})\), and \(t_j(c_{j}^{ncr}, c_{m}^{ncr})\) where \(c_{l}\) is another ncr core. We assume that the timer configurations are set based on the requirements of the application, and they are not changed during application execution. Moreover, the timers are private to the core; hence, their values are not communicated to other cores.

The shared snooping bus uses time-division-multiplexing (TDM) to arbitrate accesses to the shared memory between cores. cr cores are pre-assigned one TDM slot while ncr cores are granted access to the shared bus during TDM slots that have no pending request from cr cores, which we call slack slots. The TDM bus arbitrates memory requests, data responses, and coherence messages. We assume the TDM slot-width \(SW\) to be large enough to complete one data transfer from the shared memory to the private cache of a core, and the transfer of any necessary coherence messages. The transfer of coherence messages and data responses begin at the start of a TDM slot. We also assume that a core can issue only one memory request in its designated TDM slot.

V. Motivating Examples

Cache coherence maintains a coherent view of multiple copies of shared data by systematically propagating changes of one copy to the other copies. In conventional cache coherence protocols [16], the propagation of changes occurs independent of the criticality of the core that either has a valid copy of the data or requests it. Therefore, current coherence techniques do not provide a mechanism to distinguish accesses from cr
cores over ncr cores. Even the state-of-the-art cache coherence protocol in real-time systems called PMSI [3] assumes all cr cores. The ability to identify requests from cr or ncr cores is essential in DCMSs. This is because a key principle in DCMS is to reduce the interference suffered by cr cores originating from ncr cores to assist in tighter worst-case bounds while encouraging ncr cores to meet its bandwidth requirements.

PMSI [3] does not differentiate criticality of cores. Therefore, a ncr core in PMSI would be treated as a cr core. This means the coherence state of a shared cache line of a cr core is affected by the activities of the ncr core by the mere fact that a TDM slot must be assigned to the ncr core. Consequently, we find that introducing criticality-awareness in cache coherence can provide tighter worst-case bounds for cr cores. An alternative is to modify PMSI to support different criticality levels. Suppose that we change the bus arbitration policy to operate as presented in Section IV. The bus arbitration presented is criticality-aware. In contrast to TDM as used in PMSI, this arbitration does not require pre-allocated slots to ncr cores as their requests are only serviced when the cr cores do not generate memory requests.

Using Figure 1a, we illustrate that this implementation allows for tighter worst-case latency (WCL) bounds for cr cores. For the sake of simplicity, we assume that PMSI also supports cache-to-cache transfers between cores, which it originally does not as presented by Hassan et al. [3]. We assume a dual-critical multi-core system of cr cores cfr and ccr, and ncr cores cncr and ncr. We only show the core activity for cr core cfr and ncr core cncr. Initially, cfr has data A in modified state 1. At 2, cncr has a write request. Since, cfr does not have a pending memory request, the arbiter uses the slack slot to issue cncr’s write request to A 3. Since cfr has the most up-to-date copy of A, it sends the data to cncr, and invalidates its copy 4. At 5, cfr has a write request to A. At 6, cncr’s write request is placed on the shared bus, and cfr sends the up-to-date data to cncr, and invalidates its copy. At 7, cncr has a write request to A. Since, cfr does not have a pending request, the bus arbitration grants this slack slot to cncr’s pending write request, and completes its write request at 7. Note that this example performs coherence correctly, but it requires a minimum of two TDM slots to be assigned to the cr cores. With PMSI, all four cores would need to be assigned at least one slot. Although this is a simple example, it illustrates that we can obtain tighter WCL bounds on cr cores.

Note that we only ensure WCL bounds for cr cores, and no guarantees on either WCL or bandwidth for the ncr cores. However, we do wish to provide ncr cores a mechanism to improve its memory bandwidth utilization while still ensuring WCL bounds for cr cores. For example, in Figure 1a, consider that the first write request to A from cncr (2) is succeeded by multiple read and write requests to A from cncr (not shown). Currently, requests from cr cores to the same data results in cncr’s copy of A to be invalidated. This in turn results in cache misses for succeeding requests to A for the cncr. A mechanism that we investigate in this work is to allow cores to hold shared data in their private caches for a pre-defined time duration. The time duration still guarantees WCLs for cr cores, but it allows ncr cores to leverage cache hits for repeated data accesses resulting in increased memory bandwidth utilization.

Figure 1b shows the use of timers with the proposed criticality-aware bus arbitration policy. We assume that only the ncr cores have timers. The initial states (1, 2) are similar to the example in Figure 1a. At 3, cncr’s write request is satisfied in the slack slot of cfr. The difference from the previous example is that cncr holds A for a time duration of 1 TDM period. In other words, at the end of the next slot of cfr, cncr self-invalidate its copy of A in its private cache. During this time period, successive write requests from cncr to A are cache hits 5, 6 resulting in high memory bandwidth utilization. During this timer period, the response for the write request from cfr 4 is deferred until the end of the timer duration or timeout 7. At the end of the timer duration, cncr invalidate its copy of A (8), and sends it to the first pending cr core, which is cfr. Note that this reordering of memory requests between the ncr and cr cores is a valid reordering under sequential consistency [16]. Hence, timers introduce a trade-off between the WCL of memory requests from cr cores, and memory bandwidth utilization of ncr cores.
VI. HourGlass: A Time-based Predictable Cache Coherence Protocol

HourGlass is a predictable time-based cache coherence protocol for DCMSs. We derive HourGlass from the conventional MSI protocol. We design HourGlass such that there is a per request worst-case latency bound for cores. For ncr cores, there are no guaranteed bounds, but we provide means to support improved memory bandwidth. For predictability, we must satisfy the invariants described in PMSI [3] for cores, but we must also prioritize ncr cores over cr cores.

TABLE I: Different HourGlass transitions based on core criticality.

<table>
<thead>
<tr>
<th>Criticality</th>
<th>State</th>
<th>Bus events</th>
</tr>
</thead>
<tbody>
<tr>
<td>cr</td>
<td>IS²</td>
<td>update cr-Dest/IS²/</td>
</tr>
<tr>
<td>cr</td>
<td>IS¹/²</td>
<td>update cr-Dest/IM¹/²</td>
</tr>
<tr>
<td>cr</td>
<td>IM¹/²</td>
<td>update cr-Dest</td>
</tr>
<tr>
<td>cr</td>
<td>IM¹/²</td>
<td>update cr-Dest</td>
</tr>
<tr>
<td>ncr</td>
<td>IS²</td>
<td>update cr-Dest</td>
</tr>
<tr>
<td>ncr</td>
<td>IS¹/²</td>
<td>update cr-Dest</td>
</tr>
<tr>
<td>ncr</td>
<td>IM¹/²</td>
<td>update cr-Dest</td>
</tr>
<tr>
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<td>IM¹/²</td>
<td>update cr-Dest</td>
</tr>
</tbody>
</table>

A. Architectural Modifications

Figure 2 shows the architectural support necessary for HourGlass. The architectural changes can be categorized into modifications to the shared bus (Section VI-A1), and modifications to the cache controllers (Section VI-A2).

1) Architectural modifications to shared bus: Recall that we assume a criticality-aware arbitration scheme with cr and ncr cores. The arbitration assigns slots to only cr cores, and services ncr cores in slack slots. Hence, we assume the hardware support to arbitrate across cr cores, and service requests during slack slots or during assigned slots is already available in the shared bus. Since HourGlass is criticality-aware, this requires support to identify and reorder core destinations for cache-to-cache transfers and self-invalidation messages based on the criticality of the requesting core. For example, consider cr⁰ that has a modified copy of a cache line in its private cache. Further, consider two pending requests to the same cache line from ncr⁰ and cr¹ that are observed in the same order by cr⁰. We require HourGlass to identify and reorder data responses such that cr⁰ sends the data to cr¹ first, and cancels the pending data response to ncr⁰ although it observed the request from ncr⁰ first. To support this, we add a pending response (PRSP) buffer for each core in the shared bus that holds coherence messages related to sending data to another core and to the shared memory, and self-invalidation messages (explained in Section VI-B) from cores after their timers expire. This is shown as 1 in Figure 2. Each PRSP buffer is of size N. The arbiter identifies canceled pending data responses from ncr cores in the presence of data responses to cr cores. This is done using a valid bit in the PRSP entries shown in 1.

Adding PRSP buffers requires changes to the criticality-aware arbitration logic. Cache-to-cache transfers, write-backs to shared memory, and self-invalidations due to coherency in HourGlass are carried in the TDM slot of the remote core requesting the data or causing the self-invalidation. Hence, at the start of a TDM slot for a particular core c_k, the arbitration logic must index the PRSP buffers of all the cores to identify if there are pending cache-to-cache data responses with destination core as c_k or self-invalidation responses for c_k. If there exists one, the data response to c_k or self-invalidation is carried out in the TDM slot for c_k. If c_k does not have a pending request, and no data responses or self-invalidation messages for c_k exist in the PRSP buffers of other cores, this TDM slot is assigned to a ncr core (slack slot) in round-robin. The arbiter determines which ncr core to grant access to the bus at the beginning of the slack slot, and only ncr core may proceed. This ensures that the ncr core can complete within the slot.

2) Architectural changes to cache controllers: HourGlass uses timers to guarantee WCL bounds for cr cores while simultaneously allowing ncr cores to receive improved memory bandwidth. These timers are typically available in most current commercial-off-the-shelf (COTS) micro-architectures in the form of time-stamp registers. For example, x86 architectures have the timer-stamp registers [17] that increments based on the core frequency, and most ARM architectures have a system counter that counts at a specific frequency [18]. We employ such high precision timers for HourGlass.

In order for cores to hold cache lines for a time duration, we extend the tag bits of cache lines to hold two timer values for each core, and service requests for cr cores, and service requests during slack slots or during assigned slots is already available in the shared bus. Since HourGlass is criticality-aware, this requires support to identify and reorder core destinations for cache-to-cache transfers and self-invalidation messages based on the criticality of the requesting core. For example, consider cr⁰ that has a modified copy of a cache line in its private cache. Further, consider two pending requests to the same cache line from ncr⁰ and cr¹ that are observed in the same order by cr⁰. We require HourGlass to identify and reorder data responses such that cr⁰ sends the data to cr¹ first, and cancels the pending data response to ncr⁰ although it observed the request from ncr⁰ first. To support this, we add a pending response (PRSP) buffer for each core in the shared bus that holds coherence messages related to sending data to another core and to the shared memory, and self-invalidation messages (explained in Section VI-B) from cores after their timers expire. This is shown as 1 in Figure 2. Each PRSP buffer is of size N. The arbiter identifies canceled pending data responses from ncr cores in the presence of data responses to cr cores. This is done using a valid bit in the PRSP entries shown in 1.

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will have two countdown timers \( t_i(c_{cr}^i, c_{ncr}^i) \) (ncr timer) and \( t_i(c_{cr}^j, c_{ncr}^j) \) (cr timer) where \( i, j, k \in \{0, ..., N - 1\} \). The initial values of the countdown timers are computed based on the TDM slot width. We assume that the counter values are represented as 64 bit values. This architectural modification is shown in Figure 2 as ①. When a core receives a cache line from either the shared memory or from a remote core, the timer values are set with the timeout configured values, and begin to count down every cycle until they are zero.

We augment the cache controller with logic to identify the criticality of remote requests. We assume that cores are aware of the criticality of other cores present in the multi-core platform. This information can be configured at boot time, and stored in a dedicated on-chip read-only memory (ROM). The criticality of the requesting core is identified through the coherence messages (explained in Section VI-B). This allows a core that holds a valid copy of a cache line to differentiate the criticality of pending memory requests. The ability to differentiate criticality of pending memory requests is necessary for cache-to-cache transfers. This is because in the event of multiple pending requests for different critical cores to a cache line, the core that sends the cache line must send the data to the oldest pending core. To this end, we further extend the tag bits of a cache line to include two destination fields to denote the cr- and ncr cores requesting the cache lines as shown in Figure 2 as ②. Hence, if both destination fields for a cache line have valid core identifiers, the cache line will be transferred to the core. Note that once a destination field is populated with a valid core identifier, it is not overwritten with another core identifier. This is done in order to service multiple pending requests to a cache line from the same criticality cores in a predictable manner.

We also track accurate information about the sharers of cache lines in the system at the shared memory (more details in Section VI-B). This is not necessary in conventional cache coherence protocols, and PMSI. Hence, the cache lines of the shared memory are extended by sharer bits that track the sharers of a cache line. This is shown as ③ in Figure 2. The maximum number of sharer bits is equal to the number of cores in the multi-core platform. This is because multiple cores can have a cache line in the shared state (S), and timeout at different instances as each core may have received a copy of the cache line at different time instances. Knowledge about when no cores in the system have a valid copy of the data is important to HourGlass in order to avoid data incoherence. We explain this in detail in Section VI-B. HourGlass requires modifications to the pending request lookup table (PR LUT) in the shared memory. The PR LUT is an implementation of an invariant listed by Hassan et al. [3] for building predictable cache coherence protocols. The PR LUT manages multiple pending requests to the same cache line in a predictable manner. With support for criticality, we require modifications to the PR LUT such that pending requests from cores to a cache line are serviced before ncr cores to the same cache line. Hence, we extend the PR LUT to include the criticality of the pending requests to a cache line shown as ④ in Figure 2, and add logic to cancel pending ncr requests to a cache line on encountering a request to the same cache line by a core. Section A-D describes the hardware overhead of HourGlass for a four core system.

### B. Coherence Protocol Modifications

HourGlass requires modification to the MSI cache coherence protocol in addition to the architectural changes listed earlier for criticality awareness. This is because coherence messages and responses need to be differentiated based on the criticality of the cores. Tables I and A1 describe the different coherence states and transitions between states for the private caches. Core events denote activities of the core such as loads, stores, and replacements, and bus events denote coherence messages and data responses observed on the bus. We categorize the changes to MSI into two categories: changes for criticality awareness, and changes for timer support.

1) Changes for criticality-awareness: Recall from Section VI-A that the cache controllers have hardware support to differentiate memory requests from different criticality cores. This differentiation is carried out through the coherence messages sent by remote cores. Since each core is aware of the criticality of the other cores in the system, the core identifier information in coherence messages from remote cores is used to identify their criticality. Hence, we introduce two classes of coherence messages based on the criticality of the remote core denoted as Message-cr, and Message-ncr. For example, OtherGetM-cr denotes that a core with a valid copy of a cache line sees a store request from a core.

The shared memory identifies cache lines that are not cached in the private caches of cores (I state), and when there exists at least one core with a valid read-only copy (S). In the conventional MSI cache coherence protocol and PMSI, the shared memory fuses the I and S states into one I/S state. This is necessary in order to track multiple sharers of a cache line that can timeout at different time instances. The shared memory also has information about the criticality of cores present in the system. This is necessary when the shared memory sends data responses to requesting cores. For example, if a core has a read request to a cache line, and no other cores have a modified version of the cache line, the shared memory is responsible for supplying the data.

2) Support for Timers: Timer support in HourGlass also requires changes to the coherence protocol as timers allow cores to hold cache lines for a duration of time. We introduce new stable and transient coherence states to accommodate timer support in HourGlass. When a core receives data either from a remote core or from the shared memory, it moves to a stable state (S or M state), and populates both timer fields with timeout values, and begins to count down. When a core in a valid stable state such as shared (S) or modified (M) observes a request from a remote ncr- or cr-core, it moves to a stable state S^{T1} or M^{T1}, respectively. These states indicate that pending remote requests are observed by the core with a valid copy of the cache line, but the responses to these remote requests are deferred until timers timeout. Once
the timers expire, the core issues a SelfInv or SendData coherence message to indicate that the core is either ready to selfinvalidate its valid copy of the data or send the data to the requesting core. As a performance optimization, we add support for restarting timers if a core with a valid copy of the cache line does not observe remote write requests. These coherence messages contain the remote core identifier and its criticality information. The PRSP buffer introduced in Section VI-A holds these coherence messages and their information to allow the shared bus for canceling coherence responses from ncr cores in the presence of responses from cr cores. As mentioned in Section VI-A, these messages are issued by the bus arbitration in the TDM slot of the requesting core, which is available in the coherence message.

To avoid breaking the illusion of the single writer multiple reader (SWMR) invariant, which is an important property of cache coherence protocols, we introduce the coherence message AllInv that is generated by the shared memory once all sharers have self-invalidated their copies of a cache line. Consider the following scenario where cores $c_i^{cr}$ and $c_j^{ncr}$ have valid copies of a cache line in shared ($S$) state, and $c_i^{cr}$ has a pending write request to the same cache line. The pending write request needs to be satisfied after all sharers have self-invalidated their copies of the cache line. If the pending write request is satisfied otherwise, the system will result in at least two copies of the cache lines existing in the shared ($S$) state and modified ($M$) state simultaneously breaking the SWMR requirement. Hence, SelfInv messages sent by the sharers are observed by the shared memory, and the sharer information in the shared memory is updated accordingly. Once all the sharers of a cache line have self-invalidated, the shared memory issues the AllInv coherence message, which indicates updates to the cache line can proceed safely. Note that HourGlass currently does not allow for upgrades, which are optimized transitions from $S$ to $M$, and it does not allow a cache line in $M$ to move to $S$ state. For a cache line to move from $S$ to $M$ state on a write request, it has to wait for its own timer ($t_i(c_i^{cr}, c_i^{cr})$) or $t_i(c_j^{ncr}, c_j^{ncr})$) to timeout before proceeding with the write request. Section A-A presents an example that shows how HourGlass handles multiple pending requests from cr and ncr cores.

### VII. Timing Analysis

We derive the worst-case (WC) latency bound of a memory request, $L_i$, that a critical core, $c_i^{cr}$, suffers due to interference from other cores upon accessing the shared cache hierarchy. $L_i$ has three latency components: arbitration (Definition 1), basic access (Definition 2), and coherence (Definition 3).

**Definition 1.** *Arbitration latency*, $L_{i,arb}^{cr}$, of a request $r$ generated by $c_i^{cr}$ is measured from the timestamp of its issuance until it is granted access to the bus. $L_{i,arb}^{cr}$ occurs due to prior requests from other cores scheduled before $c_i^{cr}$.

**Definition 2.** *Access latency* is the time required to transfer the requested data by $c_i^{cr}$ from the shared memory to the private cache of $c_i^{cr}$. We assume that the data transfer takes a fixed latency, $L_{acc}$.

**Definition 3.** *Coherence latency*, $L_{coh}^{i,r}$, of a request $r$ generated by $c_i^{cr}$ is measured from the timestamp when $r$ is granted access to the bus until it starts its data transfer. $L_{coh}^{i,r}$ is due to the coherence protocol rules that ensure data correctness in the cache hierarchy.

A request generated by $c_i^{cr}$ to a cache line $A$ suffers a coherence latency in three situations:

1. If another core, $c_j$, (critical or non-critical) has $A$ in a modified state. Thus, $c_i^{cr}$ has to wait until $c_j$’s timer for $A$ expires before it gains access to it.
2. If $C$ critical cores requested $A$ to be modified before $c_i^{cr}$ issued its request, where $C \geq 1$. In this case, $c_i^{cr}$ has to wait for $C$ cores to perform its operations and wait for its timers to expire before $c_i^{cr}$ gets access to $A$.
3. If $c_i^{cr}$ has $A$ in shared state and wants to write to it. In this case, $c_i^{cr}$ must wait for $A$’s timer to expire in its private cache before $c_i^{cr}$ issues its own write request to $A$.

**Lemma 1.** The WC arbitration latency of any request generated by a critical core $c_i^{cr}$ can be calculated as:

$$WCL_{i,arb}^{cr} = N_{cr} \times SW$$

**Lemma 2.** The WC coherence latency, $WCL_{coh}^{i,r}$, for a request issued by $c_i^{cr}$ to a cache line $A$ occurs under the following critical instance.

1. $c_i^{cr}$ issues a write request to $A$, which $c_i^{cr}$ has just received to be in the shared state in its private cache.
2. Afterwards, before the expiration of $A$’s timer in $c_i^{cr}$’s private cache, a non-critical core $c_j^{ncr}$ obtains $A$ in the shared state.
3. Before $c_j^{ncr}$ times out, another critical core $c_k^{cr}$ requests $A$ in the modified state. Hence, $c_k^{cr}$ has to wait for $v(n_{cr}, cr)$ for $c_j^{ncr}$ to time out. In addition, the self-invalidation message of $c_j^{ncr}$ will be issued in $c_k^{cr}$’s slot, which in the worst-case will have to wait for $N_{cr} - 1$ slots.
4. Finally, in the period between action 2) and the expiration of $A$’s timer in $c_k^{cr}$’s cache, all other ($N_{cr} - 1$) critical cores issue write requests to $A$.

Accordingly, its WC coherence latency is:

$$WCL_{i,coh}^{cr} = v(cr, cr) + v(n_{cr}, cr) + ((N_{cr} - 1) \times SW) - (N_{cr} - 1) \times SW)$$

We present the proof for this lemma in Section A-B.

**Theorem 1.** From Lemmas 1 and 2, and given that the access to the cache takes one TDM slot of SW cycles, the total WC latency of a request by $c_i^{cr}$ is as follows.

$$WCL_{i, tot} = WCL_{i,arb}^{cr} + WCL_{i,coh}^{cr} + L_{acc}$$

**Proof.** The total WCL is the summation of the arbitration, access, and coherence latencies.

\[ \square \]
VIII. Evaluation

We implement HourGlass\(^1\) in gem5 [4], which is a cycle accurate micro-architectural simulator. We use the Ruby memory model to implement the cache, memory subsystem, and coherence protocol with high precision. Our multi-core setup consists of four x86 inorder cores that run at 2GHz. We use two \(c_r\) cores \(c_{0r}, c_{1r}\), and two \(n_r\) cores \(c_{2r}, c_{3r}\). Every core has a separate 16kB direct mapped private L1-data (L1-D) and instruction (L1-I) cache with a cache line size of 64B. We use a 3 cycle access latency to the private L1 caches. All the cores share a 8-way 1MB set-associative last-level cache (LLC). Accesses to the LLC are assumed to be perfect and incur an access latency of 50 cycles. This allows our evaluation to focus on measuring metrics relevant to cache coherence. We assume that main-memory access overheads can be calculated using prior approaches such as [19], and are additive to the coherence latencies derived in this work [20]. The bus manages accesses between cores to the shared memory using the policy described earlier. For our evaluation, we use SPLASH-2 [5] as a multi-threaded benchmark suite, and multi-threaded synthetic benchmarks for maximum sharing of data across cores. We run these benchmarks using four threads, and we map each thread to a core.

A. Data and Protocol Verification

We verify the correctness of HourGlass using synthetic and SPLASH-2 benchmarks. The synthetic benchmarks exercise maximum sharing of data by executing the same set of instructions across all cores on the same data. With these, we manually verify that all state transitions, and timer events of HourGlass are correctly exercised. This confirms correctness of HourGlass. For data correctness of HourGlass, we check the output of SPLASH-2 benchmark suite. These benchmarks have in-built single threaded verification routines that check the output generated from the multi-threaded workload.

B. Bounding memory access latencies

We show that with HourGlass, \(c_r\) cores have a bound on the access latency to shared data. Figure 3 shows the observed worst-case request access latency, and the individual latency components such as the coherence latency, and arbitration latency for the \(c_r\) cores using SPLASH-2 and synthetic benchmarks. In this evaluation, we configure the initial timer values as follows: \(v(c_r, c_r) = 2\ast TDM\), \(v(c_r, n_r) = 4\ast TDM\), \(v(n_r, c_r) = 1\ast TDM\), and \(v(n_r, n_r) = 2\ast TDM\).

We observe in Figure 3 that the WCL for all benchmarks, and their respective components are within the analytical bounds. We note that SPLASH-2 is designed such that there is minimal data sharing across multiple threads. Hence, the observed WCLs in Figure 3a for the different components are also well within the analytical bounds. Figure 3b shows that WCL of \(c_r\) cores using synthetic benchmarks that perform the same set of instructions all cores. We observe that for synthetic workloads that stress the coherence protocol, the WCL are within the analytical bounds.

C. Comparison with PMSI

Figure 4 shows the WCL of a memory request from \(c_r\) cores and \(n_r\) cores deployed using HourGlass and PMSI. The PMSI protocol is modified to support cache-to-cache transfers, and hence we compute the analytical WCL for a memory request under this variant of PMSI accordingly. We also compare with a HourGlass configuration that sets the initial timer values to zero (HourGlass \((0,0,0,0))\). For this evaluation, we use one of the synthetic benchmarks (Synth1) that stresses the worst-case scenarios for both protocols.

When the timer values are zero, HourGlass provides tighter bounds on the WCL of \(c_r\) cores compared to that of PMSI. This is because the criticality-aware bus arbitration policy guarantees slots only for \(c_r\) cores resulting in lower arbitration latencies. Moreover, by setting the timer values to zero, the WCL of \(c_r\) cores is further reduced. The mixed timer configuration of HourGlass has the same WCL bound for \(c_r\) cores compared to PMSI. This is because the timer configurations affects the WCL of \(c_r\) cores. On the other hand, PMSI does not differentiate between different critical cores, and hence the WCL of a memory request incurs additional arbitration latency for arbitrating across \(n_r\) cores. Another consequence of the criticality aware arbitration is the increase in WCL of \(n_r\) cores in HourGlass compared to PMSI. WCL of \(n_r\) cores with PMSI have the same WCL of \(c_r\) cores as it does not differentiate criticality of memory requests. HourGlass on the other hand grants slots to \(n_r\) cores in slack slots of \(c_r\) cores, which is dependent on the application.

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\(^1\)https://git.uwaterloo.ca/caesr-pub/hourglass
suffers a slowdown of 2.55× compared to the MESI protocol. PMSI protocol outperforms previous real-time approaches as it allows for multiple copies of shared and private data to be cached in the private caches. Hence, PMSI experiences less average slowdown (48%) compared to the previous approaches. We observe that HourGlass with criticality-awareness (HourGlass (2,4,1,2) and HourGlass (1,1,1,1)) configurations performs slightly better compared to PMSI protocol. In particular, HourGlass (1,1,1,1) improves execution time by 2% on average over PMSI. We observe that almost all SPLASH-2 benchmarks partition the data across cores such that there is minimal sharing, and have high data reuse resulting in high cache hit rates. Hence, we observe that there are abundant slack slots for ncr cores to satisfy their memory requests. Moreover, the SPLASH-2 benchmarks include synchronization of threads in the form of barriers that result in ncr cores waiting for ncr cores to satisfy the synchronization condition. This combination results in comparable execution times between HourGlass and PMSI for the SPLASH-2 benchmark suite. The HourGlass (1) configuration that considers all cores to be cr cores also performs better than the alternative real-time approaches. However, compared to previous HourGlass configurations and PMSI, this configuration experiences more slowdown compared to the MESI protocol. In particular, HourGlass (1) incurs on average a 20% and 19% increase in execution time compared to the HourGlass (2,4,1,2) configuration and PMSI, and experiences an average slowdown of 75% compared to the MESI protocol. Although SPLASH-2 benchmarks exhibit data reuse and locality, the data reuse do not occur within the timer duration. Hence, cores hold on to cache lines within a duration where they may not be reused, and unnecessarily stall cores requesting for the same cache line. This is exacerbated with calls to synchronization routines in SPLASH-2 benchmarks resulting in increased slowdown for this configuration.

E. Effect of timers on bandwidth utilization of ncr cores

For DCMS, timing guarantees are necessary only for cr cores. ncr cores on the other hand do not have timing guarantees but it may be desirable to improve their memory bandwidth utilization. This is because applications running on ncr cores may have high locality and hence high execution throughput. We observe that with HourGlass, varying memory

**TABLE II: HourGlass configurations.**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Timer values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hourglass(2,4,1,2)</td>
<td>$v(c_r, c_r) = 2 \times P$, $v(c_r, ncr) = 4 \times P$, $v(ncr, c_r) = 1 \times P$, $v(ncr, ncr) = 2 \times P$</td>
<td>Different timer values based on criticality of cores that have valid copy and requesting cores</td>
</tr>
<tr>
<td>Hourglass(1,1,1,1)</td>
<td>$v(c_r, ncr) = 1 \times P$, $v(ncr, c_r) = 1 \times P$, $v(ncr, ncr) = 1 \times P$</td>
<td>Same timer values irrespective of criticality of cores that have valid copy and requesting cores</td>
</tr>
<tr>
<td>Hourglass(1)</td>
<td>$v(c_r, c_r) = 1 \times P$</td>
<td>All cores are cr cores</td>
</tr>
</tbody>
</table>

- **Fig. 4:** WCL of cr cores using HourGlass and PMSI.
- **Fig. 5:** Execution time slowdown compared to MESI protocol.

**D. Comparison with real-time approaches for managing shared data and conventional cache coherence protocols**

We compare the performance of HourGlass with conventional cache coherence protocols such as the MSI and MESI protocols, state-of-the-art real-time cache coherence protocol PMSI, and other real-time approaches for sharing data predictably in Figure 5. These approaches include uncach-shared [8] that caches only private data and accesses shared data from shared memory. Since, HourGlass is the only cache coherence protocol for DCMS, we present three different HourGlass configurations for comparison. We tabulate the configurations in Table II and their descriptions. The purpose of having the HourGlass (1,1,1,1) configuration is to observe the effect of slowdown suffered by HourGlass when all the timer values are uniform but still be criticality-aware. Such a configuration may have varying slowdowns compared to the default HourGlass (2,4,1,2) configuration based on the application. We also evaluate the HourGlass (1) configuration that does not have criticality-awareness, similar to PMSI. However, cache lines are held in the private caches of the cores for a duration of 1 TDM period. We use the SPLASH-2 benchmark suite for this evaluation, and compute the slowdown experienced by the different protocols and approaches compared to the MESI cache coherence protocol. uncach-shared has the largest slowdown compared to the rest of the approaches and protocols. On average it suffers from a 49.59× slowdown as the SPLASH-2 benchmarks exhibit data reuse. This is because every data access incurs the long memory access latency. uncach-shared performs significantly better than uncach-all as some of the private data are cache hits in the private caches. On average, uncach-shared
bandwidth utilizations can be achieved for ncr cores at the expense of increasing the WCL bound for cr cores. This is because the time duration for which ncr cores core holds data in its private cache (v(ncr, cr)) affects the WCL of the cr cores. We show the effects of varying two initial timer values v(cr, ncr) and v(ncr, cr) on the memory bandwidth utilization of ncr cores and WCL of cr cores in Figure 6. We use the Cholesky benchmark from SPLASH-2 as it has the lowest cache hit ratio across all the benchmarks.

From Figure 6a, the WCL of cr cores does not change with varying v(cr, ncr). However, we observe a decrease in memory bandwidth for ncr cores with increase in v(cr, ncr) as shown in Figure 6b. This is because v(cr, ncr) affects the time duration for which a cr cores core holds data in its private cache in the presence of pending requests from ncr cores. A high value of v(cr, ncr) defers responses to pending requests from ncr cores resulting in more opportunities for observing responses from cr cores and hence, reordering responses. Varying v(ncr, cr) on the other hand affect the WCL of cr cores, and memory bandwidth utilization of ncr cores as shown in Figures 6c and 6d respectively. In Figure 6c, higher values of v(ncr, cr) increases the WCL of cr cores. This is because a request from cr cores core to a shared data that is in the private cache of ncr cores core has to wait for a maximum of v(ncr, cr) before completing its request. However, increasing v(ncr, cr) allows ncr cores to increase cache hits on shared data cached in their private caches resulting in improved memory bandwidth. This is shown in Figure 6d. Hence, the timers in HourGlass provides both bounds on WCL for cr cores, and satisfy memory bandwidth requirements for ncr cores at the expense of increasing the WCL of cr cores.

IX. Conclusion

In this work, we present HourGlass, a predictable time-based cache coherence protocol that provides WCL bounds for cr cores in a DCMS. HourGlass also includes provisions to improve the memory bandwidth utilization for ncr cores at the expense of increasing the WCL of cr cores. Since HourGlass is criticality-aware, it provides tighter WCL bounds for cr cores compared to the state-of-the-art real-time cache coherence protocol. HourGlass exhibits similar total execution times compared to the state-of-the-art real-time cache coherence protocol, and experiences a 1.43× and 1.46× slowdown compared to the conventional unpredictable MSI and MESI protocols for SPLASH-2 benchmarks.
APPENDIX A

A. Example scenario with HourGlass

Figure 7 shows a scenario with multiple pending requests to a shared cache line \( A \) using HourGlass. The arbitration policy is critical awareness, and we presented the arbitration details for the criticality-aware arbitration policy in Section IV. Initially all cores do not have a valid copy of the cache line \( A \). The initial timeout value for all timer values is 2 TDM periods.

<table>
<thead>
<tr>
<th>Cores</th>
<th>Activity per TDM slot</th>
</tr>
</thead>
<tbody>
<tr>
<td>( c_0 )</td>
<td>Write A: 300 ( A \rightarrow ) DMP</td>
</tr>
<tr>
<td>( c_0 )</td>
<td>Read hit to A</td>
</tr>
<tr>
<td>( c_0 )</td>
<td>Own_SendData Send A: 100 to ( c_0 )</td>
</tr>
<tr>
<td>( c_0 )</td>
<td>TDM slots</td>
</tr>
<tr>
<td>( c_1 )</td>
<td>OtherGetM(ncr) A: ( M \rightarrow M' I )</td>
</tr>
<tr>
<td>( c_1 )</td>
<td>OtherGetM(ncr) A: ( M \rightarrow M' I )</td>
</tr>
<tr>
<td>( c_1 )</td>
<td>Own_SendData Send A: 100 to ( c_0 )</td>
</tr>
<tr>
<td>( c_1 )</td>
<td>TDM slots</td>
</tr>
<tr>
<td>( c_2 )</td>
<td>SendData down to 0, and issues a SendData message on the bus, and ( c_3 ) transfers the up-to-date A data to ( c_0 )</td>
</tr>
<tr>
<td>( c_2 )</td>
<td>TDM slots</td>
</tr>
<tr>
<td>( c_3 )</td>
<td>OtherGetM(ncr) A: ( M \rightarrow M' I )</td>
</tr>
<tr>
<td>( c_3 )</td>
<td>OtherGetM(ncr) A: ( M \rightarrow M' I )</td>
</tr>
<tr>
<td>( c_3 )</td>
<td>Own_SendData Send A: 100 to ( c_0 )</td>
</tr>
<tr>
<td>( c_3 )</td>
<td>TDM slots</td>
</tr>
</tbody>
</table>

Fig. 7: Example scenario with HourGlass.

At \( 1 \), \( c_3 \) has a pending write request to \( A \), which is serviced in the slack slot of \( c_3 \). Since, there are no sharers for this cache line, the shared memory responds with the data, and changes its state to \( M \). On receiving the data, the two timers for the cache lines are loaded with the initial timeout values and begin to count down. Since \( c_1 \) does not have a pending request, and \( c_2 \) has a pending write request to \( A \), the bus arbitration slot grants this slack slot to \( c_2 \) for its write request. At \( 2 \), \( c_2 \) notices the write request from \( c_2 \) on the bus, which is denoted as OtherGetM(ncr), and changes its state from \( M \) to \( M' I \). It also marks the ncr-destination field in its modified copy of \( A \) as c2(ncr). In the next TDM slot of \( c_1 \), \( c_1 \) has a pending write request to \( A \) that is serviced by the shared bus. At \( 3 \), \( c_3 \) observes \( cr \) core \( c_3 \)'s write request, and reissues its write request. At the same time \( 4 \), \( c_3 \) observes this write request, and updates the cr-destination field as \( c_3 \). Since, the state of \( A \) in \( c_3 \) is \( M' I \), and is waiting for its timer to expire, it does not respond to the request from \( c_0 \) yet. At \( 5 \), a read request from \( c_3 \) to cache line \( A \) is a cache hit. Notice that this is a cache hit because of the timer support, thereby improving the memory bandwidth utilization. In the absence of timers, the previous pending write requests to the same cache line would have resulted in \( A \)'s invalidation in \( c_3 \), resulting in a cache miss for this read request. At \( 6 \), the timer \( t_3(c_3, c_0) \) counts down to 0, and issues a SendData message with the requester core information set to that of the cr core \( c_0 \). \( c_3 \) moves from \( M' I \) to \( M' A \) state, which denotes that it is waiting for \( 2 \). This occurs if \( v(ncr, cr) < v(ncr, ncr) \). If \( v(ncr, ncr) > v(ncr, cr) \), the cache controller will look up the destination fields for the cache line and issue the SendData message based on the whether a cr core is pending or not.

B. Proof for Lemma 2

Proof. This proof is by contradiction.

1) Let the WC for \( cr \) be such that \( cr \) does not have \( A \) in its private cache. Then, \( cr \) does not have to wait until its timer expires before it issues its own write request to \( A \). This means \( cr \) no longer waits for \( v(cr, cr) \) (first term in equation 1). Therefore, the resulting latency is less than \( WCL^{coh} \). Thus, it cannot be the WC.

2) Let the WC be when \( A \) is not cached in the private cache of any non-critical core upon the expiration of \( cr \)’s timer of \( cr \). In this case, \( cr \) no longer waits; hence, the non-critical core does not issue any coherence messages \( (v(ncr, cr) + (Ncr - 1) \times SW) \) is removed.) Therefore, the resulting latency is less than \( WCL^{coh} \).

3) Let the WC be when \( N' \) critical cores issue write requests to \( A \) before \( A \)'s timer expiration of \( cr \) such that \( N' < Ncr - 1 \) where the remaining \( Ncr - N' - 1 \) cores have either no request or are requesting access to a different cache line \( B \). Therefore, \( cr \) waits for each \( N' \) core to access the data, and \( v(cr, cr) \) before \( cr \) gets access to \( A \). Since \( N' < Ncr - 1 \), \( N' \times (v(cr, cr) + (Ncr - 1) \times SW) \) is less than the value of the third term in Equation 1, and hence it cannot be the WC.

Finally, for all the other critical cores to request \( A \) before the expiration of \( cr \)’s timer, they need at least one TDM period. This justifies the subtracted term in Equation 1.

C. Scalability

![Fig. 8: Effect of scalability on WCL of cr cores.](image-url)

We analyzed the effects of varying the number of cr- and ncr cores on the WCL of cr cores. Recall that the WCL of cr cores is dependent on the number of cr cores, and independent of the number of ncr cores. Hence, varying the number of ncr cores should not affect the WCL of cr cores. We show these trends using Figure 8 where we vary the number of cr cores.
and ncr cores respectively. In Figure 8a, we vary the number of cr cores and keep the number of ncr cores to a constant, and in Figure 8b, we vary the number of ncr cores and keep the number of cr cores constant. For this evaluation, we use one of the synthetic benchmarks to distinctly highlight the trends as the synthetic benchmarks have maximum sharing of data across the cores\(^3\). In Figure 8a, the WCL of cr cores increases with increase in the number of cr cores. In particular, the arbitration latency is proportional to the TDM period, which is a function of number of cr cores, and the coherence latency depends on the timer values, which in turn are fixed in terms of TDM periods. In addition, the coherence latency increases quadratically with increase in the number of cr cores, and dominates the total coherence latency. However, from Figure 8b, the WCL of cr cores does not increase with the number of ncr cores. However, increasing the number of ncr cores may affect memory bandwidth utilization for ncr cores, as they contend for slack slots of the cr cores.

### D. Hardware overhead of HourGlass

We briefly summarize the hardware overhead for HourGlass on a 4-core system. Each cache line in the private caches are extended by 2 timer fields, and two destination fields resulting in an overhead of \(64 + 64 + \log_2(4) + \log_2(4) = 132\) bits. Each cache line in the shared memory includes the sharer bits, which for a 4-core system results in an overhead of 4 bits per cache line. Each entry in the PR LUT in the shared memory is extended by a bit to denote the criticality of the request in a DCMS. Each entry in the PRSP buffer holds the memory address for the request, the coherence message, the core identifier, and a valid bit. For a physical address space of 4GB, this results in roughly 40 bits per entry.

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\(^3\)Note that the other synthetic benchmarks show the same trends, and hence we show only one of the synthetic benchmarks. We do not show the evaluation of this experiment on SPLASH-2 benchmarks as they have minimal data sharing, and therefore, the trend lines are not as distinct as the synthetic benchmarks.