Diplexer Design Implementing Highly Miniaturized Multilayer Superconducting Hybrids and Filters

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Abstract—Multilayer superconducting quadrature hybrids for diplexer applications are reported for the first time in this paper. The hybrids employ highly miniature lumped element components embedded within four metal layers. The thin dielectric layers between the metal layers and the small feature size of the process allow for the miniaturization of lumped element capacitors and inductors. Hybrid-coupled diplexers using lumped element hybrids and filters have been developed, fabricated, and tested. A novel filter configuration that employs inter-resonator tap connections is also demonstrated for implementation in wideband filter applications. The whole integrated high Q (quality factor) diplexer is highly miniaturized being approximately \( \lambda_0/60 \) in size at a frequency of 1.0 GHz. The diplexer structures are amenable to superconductor microelectronics technology and can be integrated monolithically with a superconducting receiver on a single chip.

Index Terms—Bandpass filters, diplexers, niobium, radio receivers, superconducting filters.

I. INTRODUCTION

SUPERCONDUCTOR microelectronics (SME) technology has the potential for the realization of highly advanced programmable software radios. SME circuits can manage digital signals with clock speeds of 40 GHz. These high clock speeds also allow for a digital-radio-frequency (RF) architecture with direct conversion to 10–12 GHz [1]. RF filters are key components in the front end of the superconducting digital receiver. Fig. 1 shows the architecture for the receiver of an SME radio.

The RF signal received by the antenna passes through an RF filter and is sent to an ultralow noise bandpass analog-to-digital (ADC) converter. This architecture eliminates the need for the down conversion of the RF signal using a mixer and a local oscillator. The down conversion process is entirely digital, including the local oscillator. The digital signal is then conditioned at ultrafast speeds creating a true software radio.

An RF channelizer, which replaces the RF filter shown in Fig. 1, can improve the performance of the SME receiver. There exists a tradeoff between the bandwidth and the dynamic range of the superconducting ADC [2]. The RF channelizer can also reject unwanted signals between narrow sub-bands. The dynamic range and the spur-free dynamic range of the receiver determine whether it can deal with these unwanted signals [2]. Also, for larger bandwidths at higher frequencies, the total noise is increased which decreases the dynamic range. For these wideband applications, an RF channelizer can better manage wideband signals comprised of narrow sub-bands.

The proposed baseline design of the architecture shown in Fig. 1 uses high Q (quality factor) room-temperature filters. The availability of miniature superconducting microwave components will make it possible to integrate an RF channelizer and the receiver on a single chip.

The design and fabrication of multilayer superconducting quadrature hybrids is presented for the first time in this paper. A diplexer using the hybrid-coupled diplexer architecture shown in Fig. 2 is implemented using this multilayer process. The two channels of the diplexer have been designed with center frequencies of 1.0 and 1.15 GHz. A hybrid is designed at each of these center frequencies. The hybrid designed at 1.0 GHz has a more compact spiral inductor than the hybrid designed at a center frequency of 1.15 GHz. A channelizer comprised of two identical filters and two identical hybrids is designed for each of the two channels. A filter designed at the center frequency of the additional channel is placed at the output of the channelizer to demonstrate its application as a diplexer. One diplexer has \( f_1 = 1.0 \text{ GHz} \) and \( f_2 = 1.15 \text{ GHz} \), as shown in Fig. 2, and the other diplexer has \( f_1 = 1.15 \text{ GHz} \) and \( f_2 = 1.0 \text{ GHz} \). Because the two channels are near each other in frequency, both of these diplexer options perform well due to the bandwidth of the hybrids. The filter and hybrids are designed with the benefit of high capacitance parallel plate capacitors and compact spiral inductors allowed by the fabrication process. The diplexers are highly miniaturized with very low loss.

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II. FABRICATION PROCESS FOR SUPERCONDUCTING FILTERS

HYPRES has a niobium-based foundry with wafer processing and micromachining for superconducting integrated circuits. The fabrication process has been used to create superconducting circuits [2]–[5]. In this paper, this process is implemented in the design and fabrication of passive microwave circuits.

The process offers many possibilities for the fabrication of microwave components. The HYPRES process, as shown in Fig. 3, has ten levels consisting of thin niobium layers, resistive metal layers, insulating layers, and the niobium–aluminum oxide–niobium trilayer. A 100-nm-thick niobium ground plane (M0) is first deposited on the 150-mm diameter oxidized silicon substrate. The ground plane can be patterned and etched, and a 150-nm-thick insulating layer of silicon dioxide (SiO$_2$) is deposited over the ground plane. The M1 niobium layer is deposited next at a thickness of 135 nm.

An insulating layer of SiO$_2$, a resistive layer (R2), and another insulating layer of SiO$_2$ are then deposited. The two insulating layers both have a thickness of 100 nm, and the resistive layer is comprised of a thin layer of either molybdenum or Ti–AuPd–Ti. Another 300-nm-thick niobium layer (M2), a 500-nm-thick SiO$_2$ insulating layer, a 600-nm-thick niobium layer (M3), and a contact layer (R3) are the last four layers deposited during the fabrication process.

The superconducting nature of the niobium allows for low-loss microwave components. High Q parallel plate capacitors with high capacitance values can be designed because the SiO$_2$ layer between M0 and M1 is only 150 nm thick. Also, the minimum width of a line and the minimum spacing between lines for the M3 layer are 2.0 and 2.5 μm, respectively [6], which allows for the design of very compact spiral inductors. All of these advantages lead to the creation of highly miniaturized, low-loss multilayer microwave components.

III. FILTER DESIGN AND MEASUREMENTS

Two different types of filters are considered for design using the above fabrication process. One design takes advantage of the thin dielectric layer between two of the niobium layers to create large capacitors resulting in miniaturized filters. The other design creates a microstrip structure using the top and bottom metal layers as the microstrip conductor and ground layer, respectively.

A. Coplanar Waveguide Lumped Element Filter Design and Measurements

A three-pole lumped element filter is designed using the multilayer fabrication process for each of the two specified channels. Lumped element capacitors and inductors are designed to realize the bandpass filter. The steps to design the filter are outlined.

The filter design starts with the bandpass transformation from the low-pass prototype filter for the case of a three-pole filter. A 90° inverter is placed on either side of the middle resonator to make all of the resonators a combination of a parallel inductor and a parallel capacitor. The 90° inverter is realized by a π-network of a series capacitor and two shunt capacitors with negative capacitance. Fig. 4 shows the final lumped element design of the three-pole filter. An image of the filter layout is shown in Fig. 5.

The filter is designed to have a center frequency of 1.156 GHz with a bandwidth of 115 MHz. The capacitance values for the $C_{11}$ and $C_{22}$ capacitors are 15.8 and 25.0 pF, respectively. To
realize such a high value of capacitance, a parallel plate capacitor is designed using the M0 and M1 layers as the two parallel plates.

Given a 150-nm-thick layer of SiO$_2$, and a capacitance value of 25.0 pF, the width of a square plate can be calculated as being only 300 $\mu$m. To keep the filter compact, the series capacitors are also designed to be parallel plate capacitors.

The inductors are realized as planar meander line inductors. The simulated resonance frequency for this inductor is above 10 GHz. The simulated resonance frequency of the shunt parallel plate capacitor is 3.44 GHz.

Bridges are needed to short out undesired modes due to the connections from the parallel capacitors and inductors to the center line of the coplanar waveguide. These bridges reside on the M2 niobium layer. Vias are made through the SiO$_2$ layer complete the connection between the ground lines of the coplanar waveguides.

An image of the fabricated filter is shown in Fig. 6, and the lossless electromagnetic (em) simulation results are shown in Fig. 7. The size of the fabricated filter is only 1.81 mm by 0.65 mm. Since the circuit resides mainly on the M0 layer, transitions by vias are made from the M3 niobium layer to the M0 layer. The R3 layer is used as contact pads for wire bonds.

The circuits are immersed in liquid helium to bring the niobium to a superconducting state. The measured results are shown in Figs. 9 and 10. The estimated loss of the filter from the measured data in its passband is approximately 0.26 dB. There is a shift in the center frequency of the filter from the simulation response, which is likely due to the fabrication tolerances on either the thickness or the dielectric constant of the SiO$_2$ layer between the M0 and M1 layers. The capacitance of this dielectric layer is given as 0.277 fF/$\mu$m$^2$ $\pm$ 20% [6]. Simulation results with this error considered are shown in Fig. 8. These simulations show a shift in center frequency closer to the center frequency of the measured filter. It may be possible to adjust for fabrication tolerances by adding more metal and insulating layers to the fabrication process to create microelectromechanical systems tunable capacitors.

The wideband measurement results are shown in Fig. 10. The response is spurious free up to a frequency of 3.9 GHz. The center frequency of this spurious signal is determined by the self resonance of the lumped elements within the filter. Since the
capacitors resonate at a frequency of approximately 3.44 GHz, it is not unexpected to have a spurious signal at 3.9 GHz.

B. Microstrip Filter Design and Measurements

A miniaturized microstrip filter is designed by taking advantage of the multilayer fabrication process. A tap input is used at the input of the filter and the resonator couplings are also achieved by a tap between resonators, as shown in Fig. 11.

The coupling between resonators for this filter design can be achieved by connecting the two resonators by a wire at a certain point on the inductor. The specific point that the two inductors are tapped determines the coupling coefficient between the two resonators. By determining the magnetic and electric coupling between the two resonators, the coupling coefficient can be determined [7].

Using a lumped element model of the resonators, as shown in Fig. 12, the magnetic and electric coupling can be determined. For the case of the electric coupling, a short circuit is placed between the two resonators and the resonant frequency of the filter is determined [7].

By letting the total inductance be $L_{tot}$, the coupling coefficient becomes

$$k = \frac{L_1 + L_3}{(L_1 + L_3) + L_{tot}}.$$  \hspace{1cm} (3)

To demonstrate the design of the filter, two-pole, three-pole, and four-pole filters are designed using circuit models of transmission lines and capacitors. All filters are designed to have a center frequency of 1.2 GHz and a bandwidth of 200 MHz. The simulated insertion loss data is shown in Fig. 13.

It is noted that one transmission zero appears on the high side of passband for all three filters. This transmission zero that appears between 1.85 and 2 GHz for the different filters, is a result of the tap input coupling [8]. This resonance corresponds to a frequency due to the capacitor $C_{11}$ in series with the section of transmission line TL$_{13}$. When more resonators are added to the filter, another transmission zero is created very near the high side of the passband creating a very sharp cutoff for narrower band filters. This transmission zero is due to a resonance from the parallel combination of TL$_{13}$, TL$_{12}$, C$_{11}$, and TL$_{21}$, C$_{22}$.

This filter configuration is also amenable to wideband filter designs. From (2) and (3), it is possible to achieve wider bandwidths with a simple position of the tap. A three-pole filter, as shown in Fig. 11, is designed using a circuit simulator. The transmissions lines have an impedance of 27 $\Omega$, and the following lengths at a frequency of 1.76 GHz: TL$_{11} = 56.3^\circ$, TL$_{12} = 63.4^\circ$, TL$_{13} = 22.5^\circ$, TL$_{21} = 40.8^\circ$, and TL$_{22} = 46.5^\circ$. The capacitors have capacitances of $C_{11} = 0.13$ pF and $C_{22} = 0.69$ pF. The simulated response is shown in Fig. 14.
The filter has a center frequency of 1.76 GHz, and a percentage bandwidth of 42.6%.

A two-pole filter and a three-pole filter were designed and tested to demonstrate this novel filter configuration. The filters were fabricated using a multilayer fabrication process implementing superconducting niobium layers and silicon dioxide insulating layers. The filter is highly miniaturized and exhibits very low loss due to the implementation of the superconducting layers.

For this filter design, the M0 layer is used as the ground plane for the microstrip filter. The M3 layer is used as the top layer and the input tap and inter-resonator tap connections are made by the M2 layer with via connections between layers. The minimum width of a line and the minimum spacing between lines for the M3 layer are 2.0 and 2.5 μm, respectively [6]. A transmission line width of 4 μm is used with the dielectric height of 0.85 μm. The dielectric constant of the SiO₂ is assumed to be 4.5. This 4-μm line width results in a transmission line with a simulated characteristic impedance of 27 Ω.

A transition is made from coplanar waveguide transmission line to the microstrip filter, as shown in Fig. 15. The transmission line spiral that makes up the resonator has a line width of 4 μm and a spacing of 4 μm. Vias are made from M3 to M0 at the short circuit end of the transmission line and the interdigital capacitor. Vias are made from M3 to M2 to make the tap connections at the input and between resonators.

The two-pole filter, as shown in Fig. 16, and the three-pole filter, as shown in Fig. 17 have a designed center frequency of 1.25 GHz and a bandwidth of 100 MHz. The filters are simulated using the em simulator Sonnet, and the em simulation results of the two pole filter are shown in Fig. 18. The measured results for both filters are shown in Figs. 19 and 20. As expected, the transmission zero created by the inter-resonator tap coupling appears in the response of the three-pole filter but not the response of the two-pole filter. The position of this transmission zero is consistent with its position predicted by the em simulator. When testing the filters, connections were made with wire bonds from the chip to a coplanar waveguide transmission line on an alumina wafer. This alumina wafer was placed in a metal housing with connections to coaxial cables, as shown in Fig. 21. The coaxial cables and the metal housing were immersed in liquid helium to reach the superconducting state of the niobium. The size of each resonator is only 0.5 mm by 0.55 mm making it highly miniaturized by being only λ₀/50 in size. When the tap connection is removed, em simulations show an isolation across the filter of approximately 48 dB. The em coupling between resonators is small due to the ground plane being very close to the top metal layer.
IV. HYBRID DESIGN AND MEASUREMENTS

For multiplexer applications, lumped element hybrids allow for miniaturization and ease of design. Distributed element hybrids and manifold multiplexers are relatively large at frequencies below 10 GHz [9]. The modular design of hybrid-coupled multiplexers permits the ease in design not seen when compared to the design of manifold-coupled multiplexers. The loss associated with the lumped element components is the main disadvantage of implementing a lumped element hybrid design. Multilayer superconducting lumped element capacitors and inductors allow for a high degree of miniaturization without encountering high losses.

Two lumped element quadrature hybrids are designed using the multilayer fabrication process. Lumped element parallel plate capacitors and compact spiral inductors are designed to realize these two hybrid designs.

The fabrication tolerances need to be considered when analyzing the measured responses. For example, the capacitance of the dielectric layer between M0 and M1 is given as $0.277 \; \text{fF}/\mu\text{m}^2 \pm 20\%$ [6]. Although the hybrid designed at 1.0 GHz is smaller due to its compact spiral inductor, the effect of the kinetic inductance associated with superconducting materials would be more pronounced than in the inductor design used for the hybrid designed at 1.15 GHz.

The hybrid design [10] is based on the circuit diagram shown in Fig. 2. For the hybrid designed at 1.0 GHz, the value of $C_1$ is 3.18 pF, the value of $C_2$ is 1.31 pF, and the value of $L$ is 5.62 nH. For the hybrid designed at the center frequency of 1.15 GHz, the inductance value of $L$ is 4.85 nH and the capacitance values of $C_1$ and $C_2$ are 2.75 and 1.14 pF, respectively.

The capacitors are realized by parallel plate capacitors using the M0 and M1 niobium layers as the two parallel plates. Since the layer of SiO$_2$ between these two layers is only 150 nm thick, the capacitors are very small, needing only an area of 40 $\mu\text{m} \times 280 \; \mu\text{m}$ for a capacitance of 3.18 pF. The inductors are realized by spiral inductor designs. The inductor with an inductance of 5.62 nH has an area of only 100 $\mu\text{m} \times 400 \; \mu\text{m}$. Images of the two hybrids are shown in Fig. 22. The measured and em simulation results using the em simulator Sonnet of the hybrid designed at 1.0 GHz are given in Figs. 23 and 24, respectively.
V. DIPLEXER DESIGN AND MEASUREMENTS

The two channelizers comprised of two hybrids and two filters as shown in Fig. 2 at the two distinct center frequencies were designed, fabricated, and tested. The filters are three-pole lumped element filters [11] that were designed at the two center frequencies. Images of these channelizers are shown in Fig. 25.

The circuits are immersed in liquid helium to bring the niobium to a superconducting state. Matched 50-Ω loads are fabricated using the R2 layer of the fabrication process to connect to the load port in the diplexer design. These loads are connected by wire bond to the channelizer. The measured results of the four-port channelizer designed at 1.0 GHz are shown in Fig. 26. The desired signal passing through the channelizer is shown as $S_{11}$ in Fig. 26. The signal that would be passed on to the next channelizer in a multiplexer design is shown as $S_{21}$, and the signal sent to the 50-Ω load is shown as $S_{31}$.

The measured results of the diplexer with the hybrid-coupled channelizer designed at 1.15 GHz with the filter designed at a center frequency of 1.0 GHz at its output are shown in Fig. 27. The filter is connected by wire bonds to the output of the channelizer to create the diplexer. The two channelized frequency bands are shown as $S_{21}$ and $S_{31}$ in Fig. 27. The measured results of the diplexer with the hybrid-coupled channelizer designed at 1.0 GHz with the filter with a center frequency of 1.15 GHz at its output are shown in Fig. 28. The measured results show the benefits of using high $Q$ filters and high $Q$ lumped element components. A similar diplexer designed using complementary metal–oxide–semiconductor technology would exhibit an insertion loss of at least 20 dB.

VI. CONCLUSION

The designs of two types of filters have been shown for the implementation in a diplexer design. One filter takes advan-
tage of the thin dielectric layer between parallel plate capacitors to create highly miniaturized filters. The second filter design uses novel inter-resonator tap coupling and can be implemented in wideband filter designs. The design and fabrication of highly miniature hybrids with diplexer applications using multi-layer superconductor technologies has also been reported. Two different hybrid configurations have been designed at the two channel center frequencies. Diplexers are created by adding a filter to the output of the hybrid-coupled channelizer. The channelizers are highly miniaturized being in the order of only $\lambda_0/60$ at a frequency of 1 GHz, resulting in the first highly miniaturized, high $Q$, diplexers that have ever been reported.

REFERENCES


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