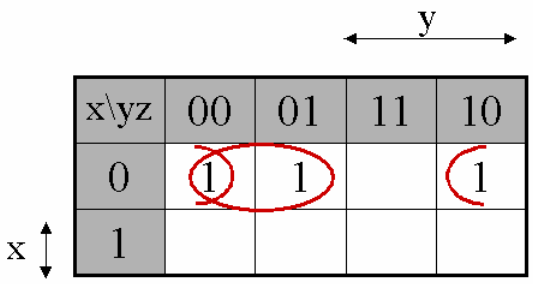
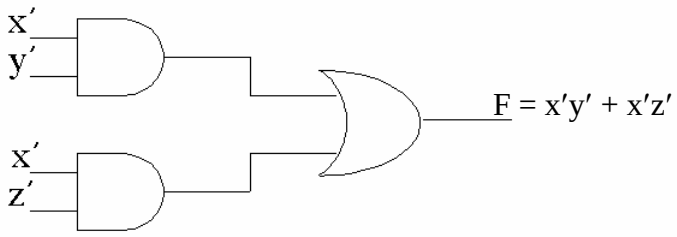
ECE-223, Solutions for Assignment #4

Chapter 4, Digital Design, M. Mano, 3rd Edition

4.4) Design a combinational circuit with three inputs and one output. The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0





4.5) Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C.
When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input.
When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

y

x\yz	00	01	11	10
0			1	
1		1	1	1

x

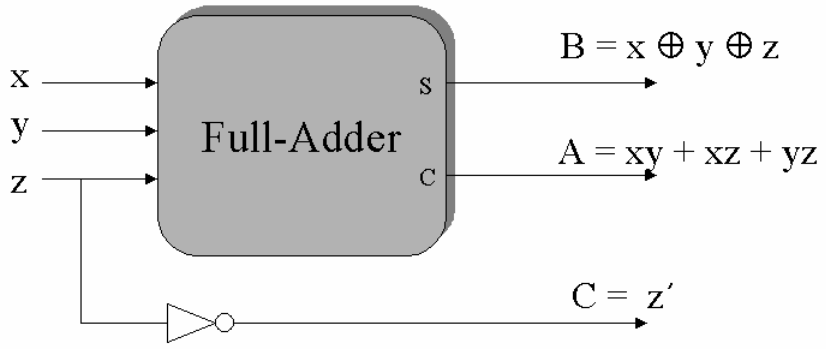
$A = xy + xz + yz$

y

x\yz	00	01	11	10
0		1		1
1	1		1	

x

$B = x \oplus y \oplus z$ $C = z'$



4.8) Design a code converter that converts a decimal digit from "8 4 -2 -1" code to BCD (See Table 1-5, Digital Design, M. Mano, pp.20)

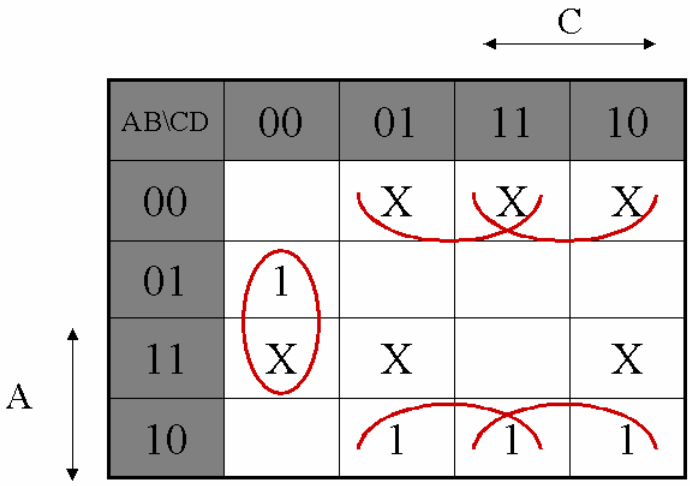
	8	4	-2	-1	8	4	2	1
	A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	1
2	0	1	1	0	0	0	1	0
3	0	1	0	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	1	0	1	1	0	1	0	1
6	1	0	1	0	0	1	1	0
7	1	0	0	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	1	1	1	1	0	0	1

C

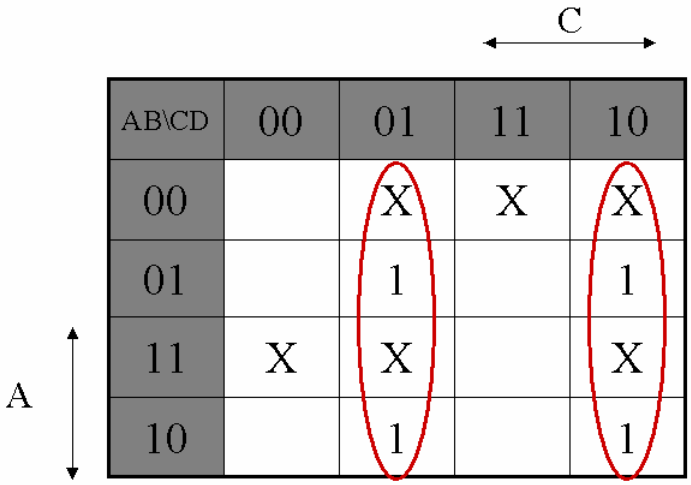
AB\CD	00	01	11	10
00		X	X	X
01				
11	X	X	1	X
10	1			

A

$$w = AB + AC'D'$$



$x = B'C + B'D + BC'D'$



$y = C'D + CD'$

and $z = D$

4.27) A combination circuit is specified by the following three Boolean functions:

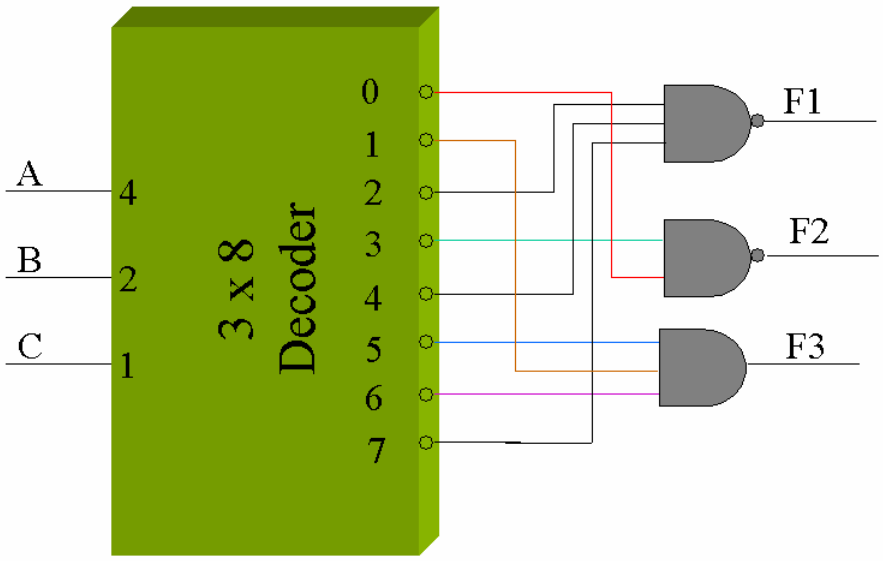
$F_1(A, B, C) = \sum (2, 4, 7)$

$F_2(A, B, C) = \sum (0, 3)$

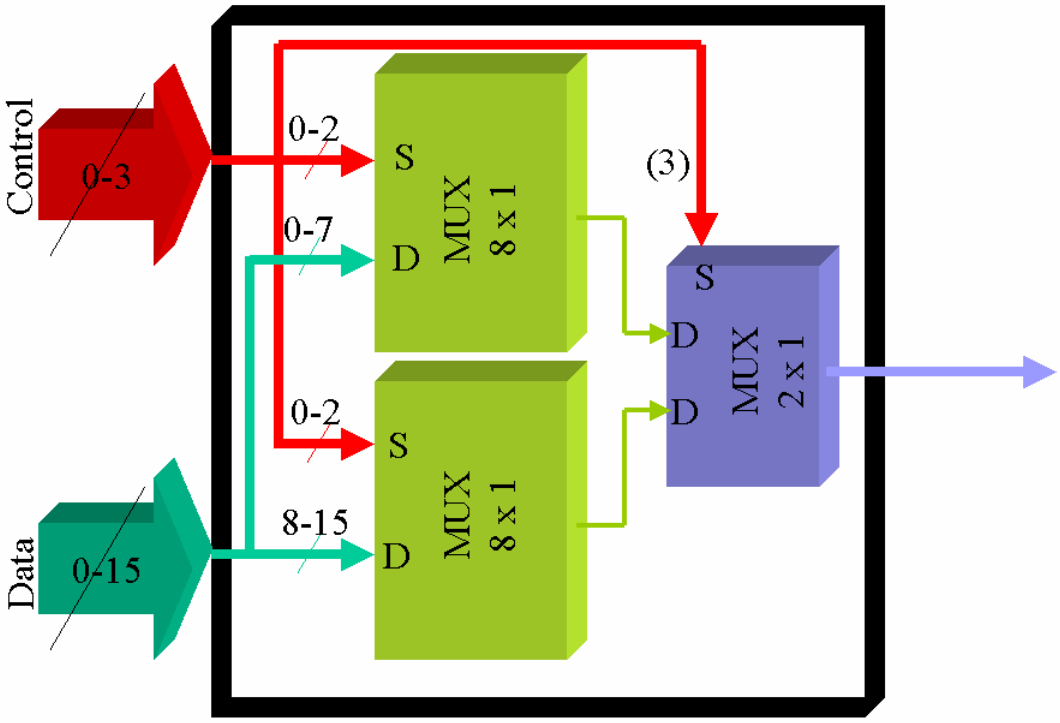
$F_3(A, B, C) = \sum (0, 2, 3, 4, 7)$

Implement the circuit with a decoder construction with NAND gates (similar to Fig. 4-19) and NAND or AND gates connected to the decoder outputs. Use block diagram for the decoder.

Minimize the number of inputs in the external gates.



4.31) Construct a 16 x 1 multiplexer with two 8 x 1 and one 2 x 1 multiplexers. Use block diagrams.



4.40) Write an HDL dataflow description of a 4-bit adder subtractor of unsigned numbers. Use the conditional operator. (?)

```
Library IEEE;
Use ieee.std_logic_1164.all;
Use ieee.std_logic_arith.all;
use ieee.std_logic_signed.all;

ENTITY add_sub IS
  PORT ( A, B :  IN    std_logic_VECTOR (3 DOWNTO 0);  -- 4-bit Data
            M    :  IN    std_logic;                                  -- M = 0 ADD ; M =1 SUB
            S    :  OUT std_logic_vector  ( 3 DOWNTO 0);     -- sum or difference
            C    :  OUT  std_logic);                                  -- Carry / Borrow
END add_sub; -- end of entity

ARCHITECTURE dataflow OF add_sub IS
 SIGNAL BM  : std_logic_VECTOR (3 DOWNTO 0);
 signal sum : std_logic_VECTOR ( 4 downto 0);

Begin
   BM <= NOT B;
   SUM  <=  ('0'&A) + ('0'&B) WHEN  M = '0' ELSE  ('0'&A)+('0'&BM)+"0001";
  S <= SUM  (3 downto 0 );
  C <= SUM  (4);
End dataflow;
```

4.41) Repeat problem 4-40 using behavioral modeling.

```
Library IEEE;
Use ieee.std_logic_1164.all;
Use ieee.std_logic_arith.all;
use ieee.std_logic_signed.all;

ENTITY add_sub IS
  PORT ( A, B :  IN    std_logic_VECTOR (3 DOWNTO 0);  -- 4-bit Data
            M    :  IN    std_logic;                                  -- M = 0 ADD ; M =1 SUB
            S    :  OUT std_logic_vector  ( 3 DOWNTO 0);      -- sum or difference
            C    :  OUT  std_logic);                                  -- Carry / Borrow
END add_sub; -- end of entity

ARCHITECTURE behavioral OF add_sub IS

 Begin

  process (A,B,M)
  variable  BM  : std_logic_VECTOR (3 DOWNTO 0);
  variable  sum : std_logic_VECTOR ( 4 downto 0);

  begin
    BM := not(B) ;
    if M = '0' then
                  sum :=  A + B;
               else
                 sum  :=  ('0'&A)+('0'&BM)+"0001";
    end if;

 S <= sum ( 3 downto 0 );
 C <= sum (4);
 end process;
End behavioral;
```