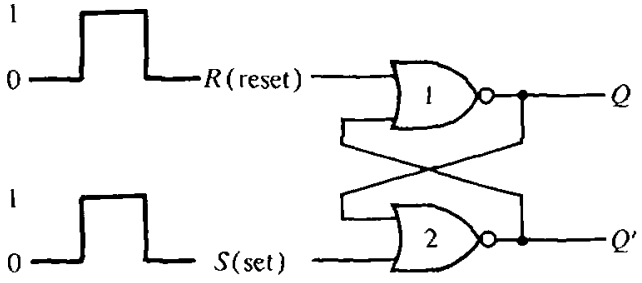
Assignment #5 E & CE 223

E&CE 223
Assignment 5 - Solutions

1: Mano 4.28

Develop truth table, and plot the Karnaugh maps.



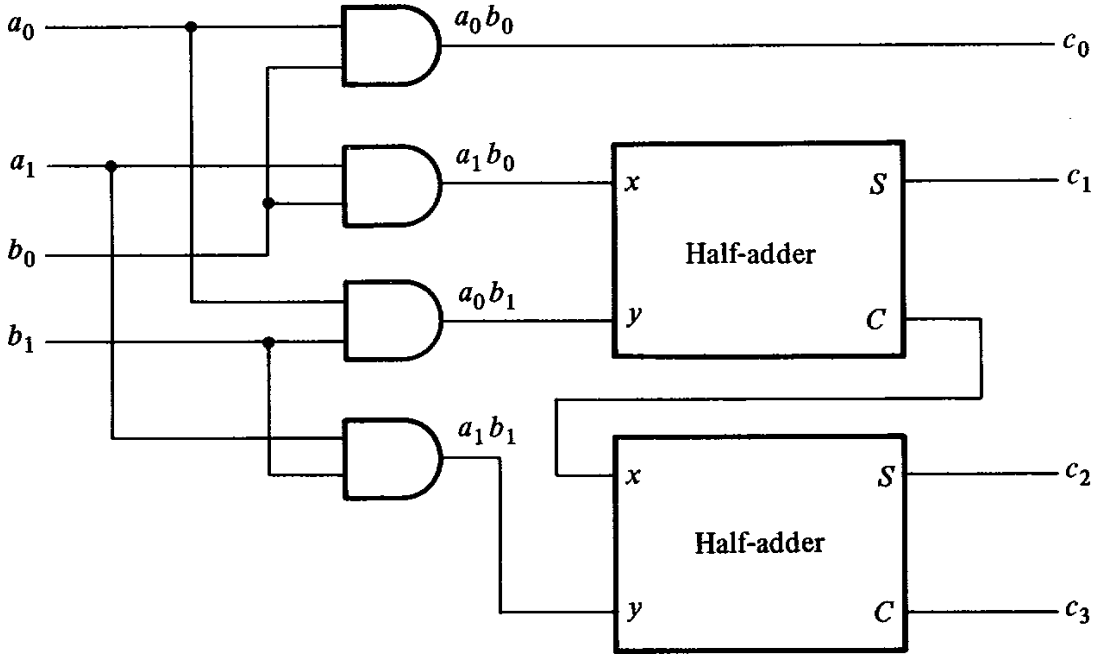
(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

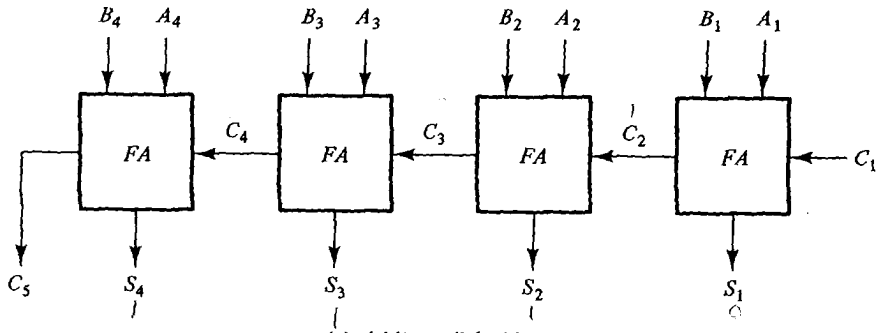
(b) Truth table

FIGURE 6-2
Basic flip-flop circuit with NOR gates

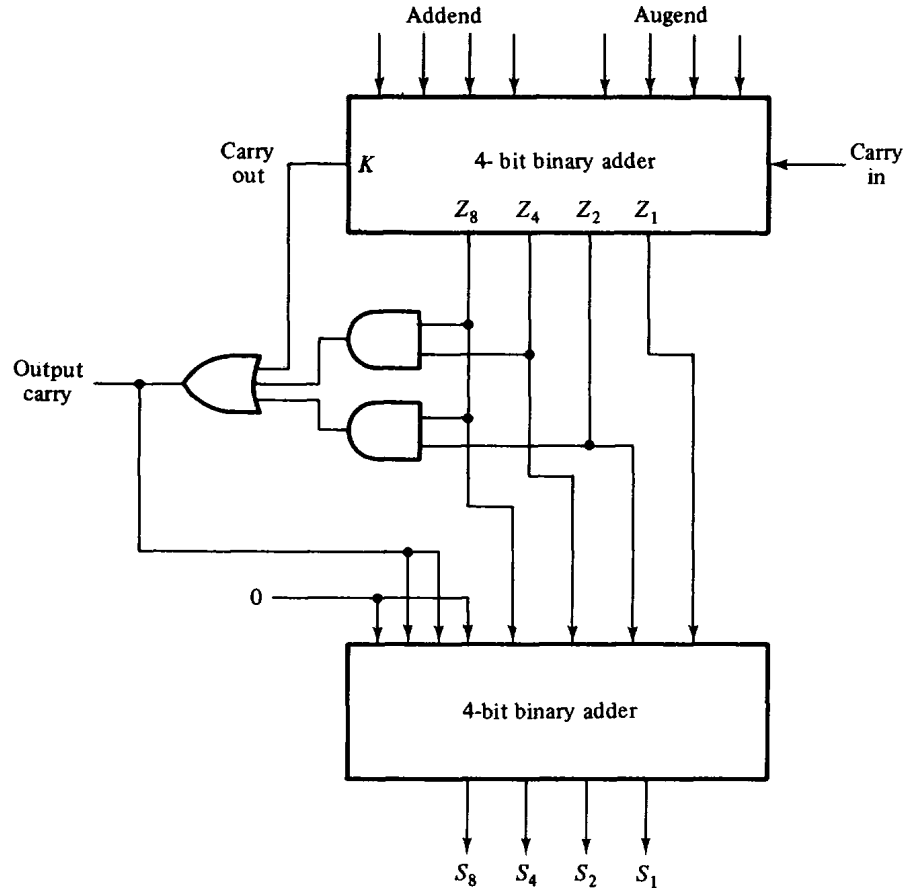
2: Mano 4.7



3: Using two four-bit adder chips, and other gates, develop a circuit for adding two BCD digits plus carry-in. Hint: If the sum is over 9 it is necessary to subtract 10 to get the BCD digit. (The circuit for a four-bit adder is shown in Figure 5-2a, page 156 of Mano.)



(a) 4-bit parallel adder



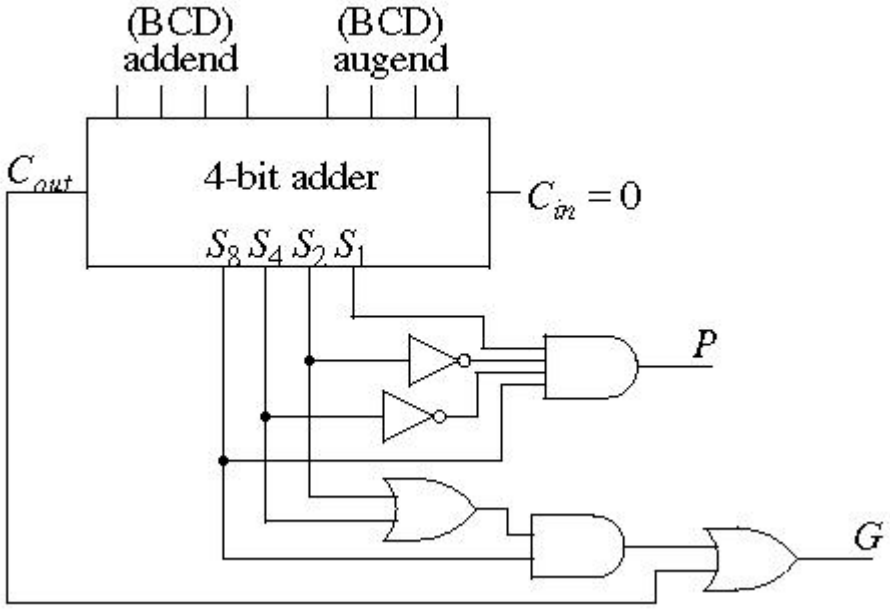
4: Develop a circuit for generating decimal "carry generate" and "carry propagate" signals for a BCD adder. Hint: Use a four-bit adder chip, and think about what output conditions represent "carry generate" and "carry propagate."

carry generate: sum > 9

$G = C_{out} + S_8 \bullet (S_4 + S_2)$

carry propagate: sum = 9

$P = S_8 S_4' S_2' S_1$



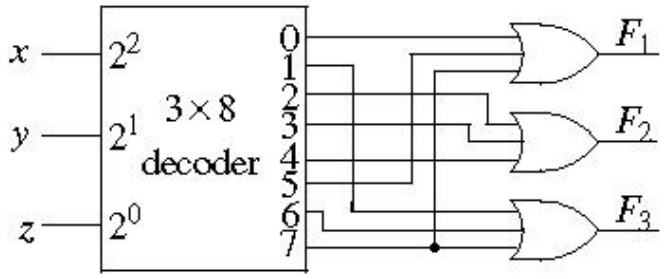
5: decoders: Mano 5.15, 5.16, 5.18

Mano 5.15

$$F_1 = x'y'z' + xz = x'y'z' + x(y + y')z = \sum(0,5,7)$$

$$F_2 = xy'z' + x'y = xy'z' + x'y(z + z') = \sum(2,3,4)$$

$$F_3 = x'y'x + xy = x'y'x + xy(z + z') = \sum(1,6,7)$$

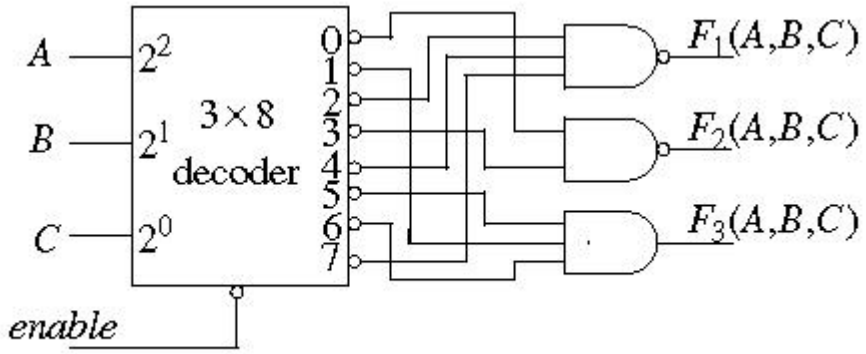


If the decoder had inverted outputs, the OR gates would be replaced by NANDs

Mano 5.16

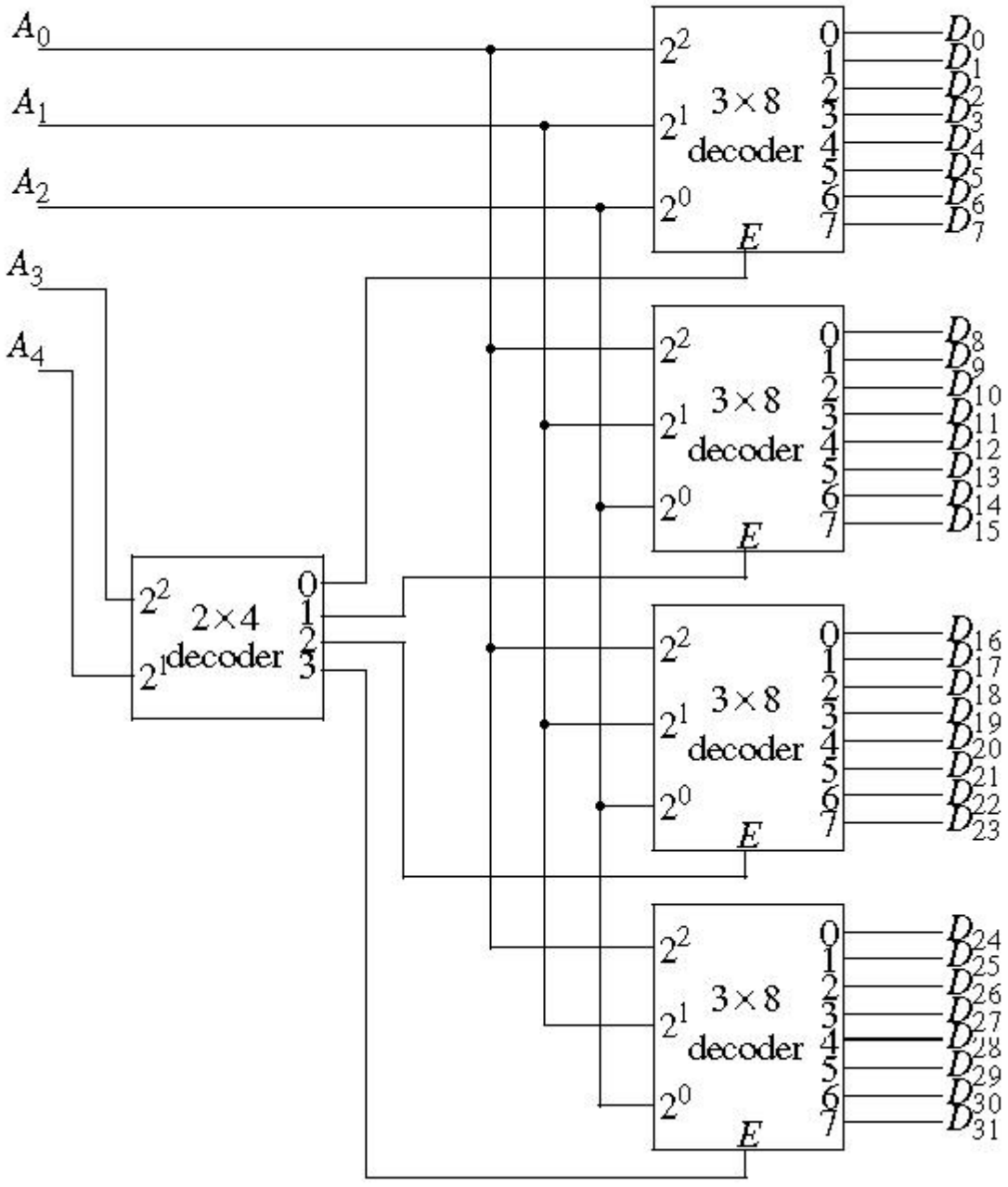
Note that

$$F_3(A,B,C) = \sum(0,2,3,4,7) = \prod(1,5,6)$$



Mano 5.18

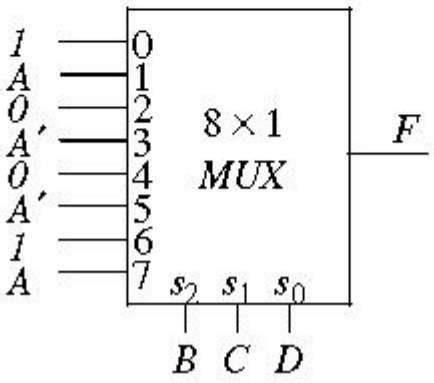
Require a 2×4 decoder to select one of four 3×8 decoders:



6: multiplexers: Mano 5.24, 5.26, 5.27, 5.28

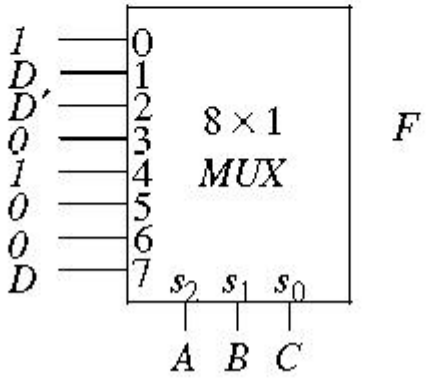
Mano 5.24

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A'	m_0			m_3		m_5	m_6	
A	m_8	m_9					m_{14}	m_{15}
	1	A	0	A'	0	A'	1	A



Mano 5.26

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
D'	m_0		m_4		m_8			
D	m_1	m_3			m_9			m_{15}
	1	D	D'	0	1	0	0	D



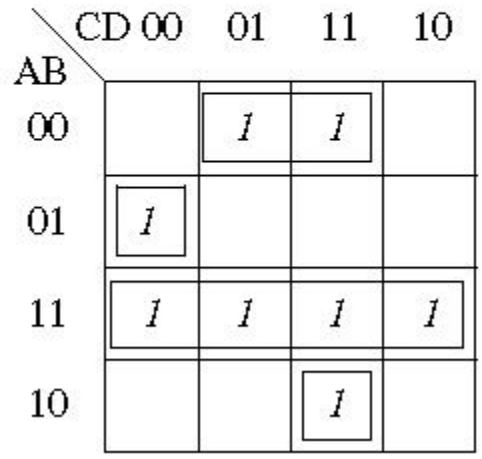
Mano 5.27

	s_2 A	s_1 B	s_0 C	D	F
$I_0 = D$	0	0	0	0	0
	0	0	0	1	1
$I_1 = 0$	0	0	1	0	0
	0	0	1	1	0
$I_2 = 0$	0	1	0	0	0
	0	1	0	1	0
$I_3 = 1$	0	1	1	0	1
	0	1	1	1	1
$I_4 = D$	1	0	0	0	0
	1	0	0	1	1
$I_5 = 1$	1	0	1	0	1
	1	0	1	1	1
$I_6 = D'$	1	1	0	0	1
	1	1	0	1	0
$I_7 = 0$	1	1	1	0	0
	1	1	1	1	0

$F(A,B,C,D) = \sum(1,6,7,9,10,11,12)$

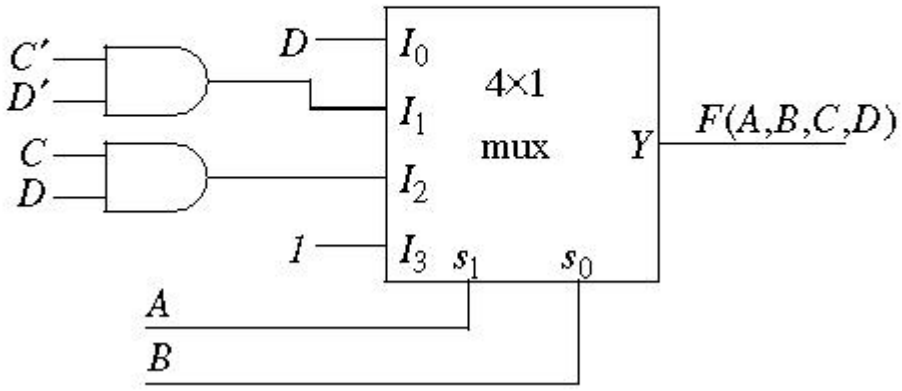
Mano5.28

$F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$



From Karnaugh map

$F = A'B'(D) + A'B(C'D') + AB'(CD) + AB(1)$

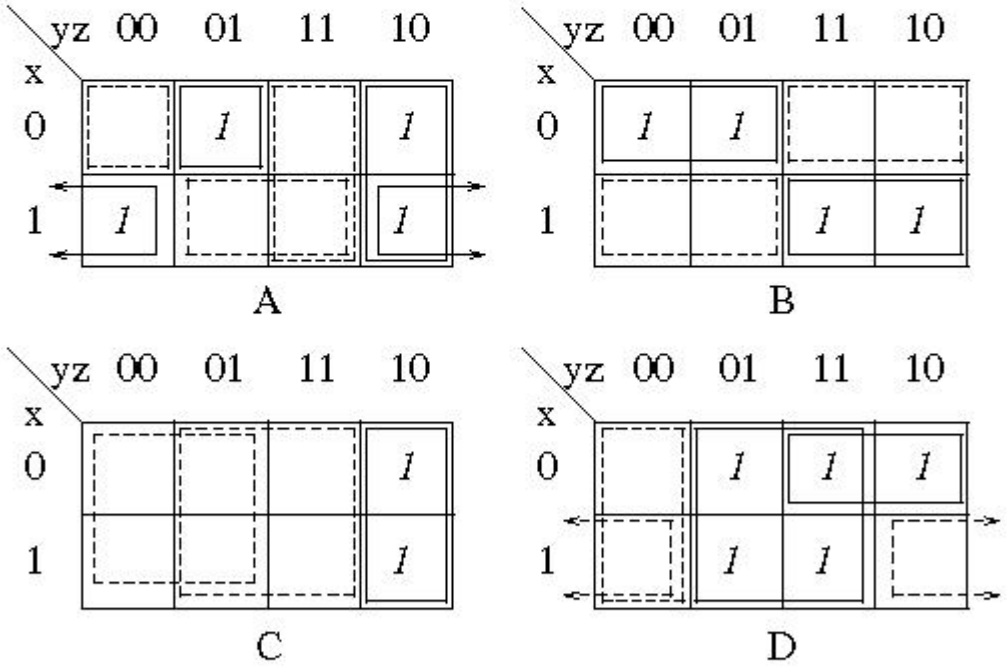


7: ROMs: Mano 5.32

input x y z	output A B C D
0 0 0	0 1 0 0
0 0 1	1 1 0 1
0 1 0	1 0 1 1
0 1 1	0 0 0 1
1 0 0	1 0 0 0
1 0 1	0 0 0 1
1 1 0	1 1 1 0
1 1 1	0 1 0 1

8: PLAs: Mano 5.33, 5.34

Mano 5.33



solid lines dashed lines

$A = x'y'z + yz' + xz'$ $A' = x'y'z' + yz + xz$

$B = x'y' + xy$ $B' = x'y + xy'$

$C = yz'$ $C' = y' + z$

$D = z + x'y$ $D' = y'z' + xz'$

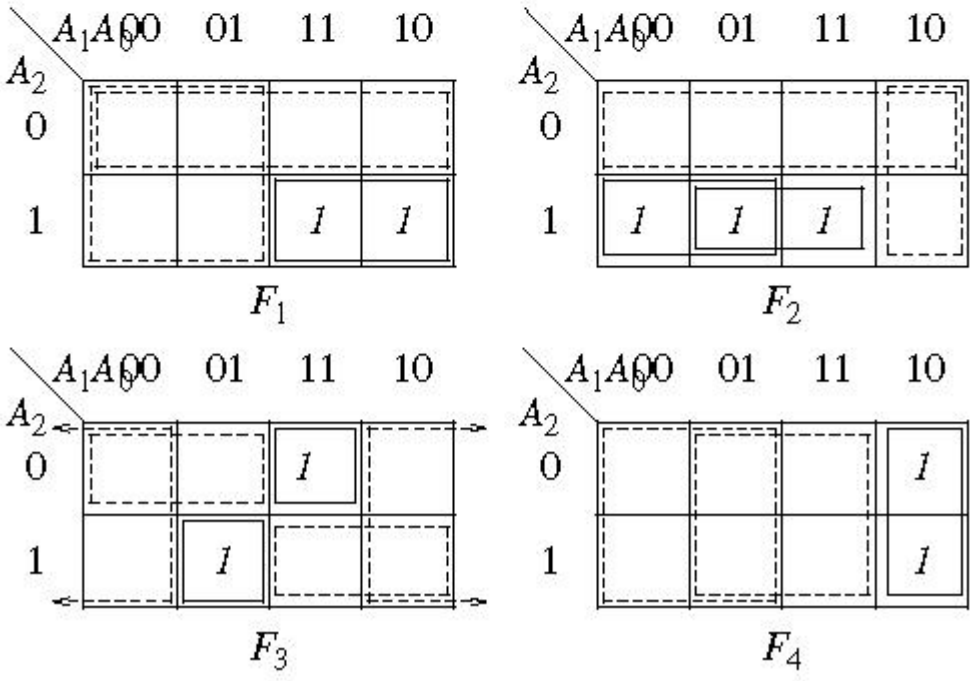
Note yz' common to A and C.
Note $x'y$ common to B' and D

		xyz	ABCD
$x'y'z$	(1)	001	1 - - -
yz'	(2)	-10	1 - 1 -
xz'	(3)	1-0	1 - - -
$x'y$	(4)	01-	- 1 - 1
xy'	(5)	10-	- 1 - -
z	(6)	--1	- - - 1
			TCTT

Another solution is:
$x'y'z$ $x'y'$ xy yz' $y'z'$ xz'

Mano 5.34

From truth table Mano Fig 5.24



solid lines	dashed lines
$F_1 = A_2A_1$	$F_1' = A_2' + A_1'$
$F_2 = A_2A_1' + A_2A_0$	$F_2' = A_2'+A_1A_0'$
$F_3 = A_2'A_1A_0 + A_2A_1'A_0$	$F_3' = A_2'A_1'+A_2A_1+A_0'$
$F_4 = A_1A_0'$	$F_4' = A_1' + A_0$

		$A_2A_1A_0$	$F_1F_2F_3F_4$
A_2A_1	(1)	1 1 -	1 - - -
A_2'	(2)	0 - -	- 1 - -
A_1A_0'	(3)	- 1 0	- 1 - 1
$A_2'A_1A_0$	(4)	0 1 1	- - 1 -
$A_2A_1'A_0$	(5)	1 0 1	- - 1 -
			T C T T

Using F_1', F_2', F_3 and F_4 also gives 5 terms.

9: Design a code converter that converts 84-2-1 code to BCD

(a) using a four input decoder,

(b) using a PLA, and

(c) using only a four-bit binary adder chip.

In all cases you may assume that only valid inputs occur.
In (b) make full use of the resulting "don't care" conditions.

From Assignment 3, Question 5 (Mano 4.13) we have:

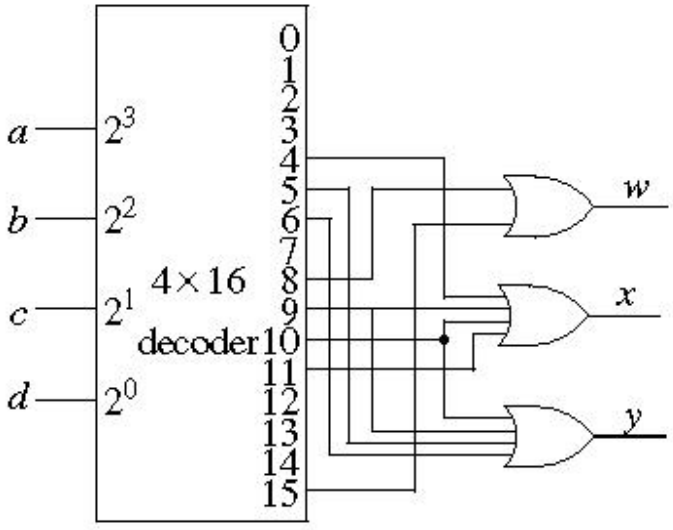
a 8	b 4	c -2	d -1	w 8	x 4	y 2	z 1
0	0	0	0	0	0	0	0
0	0	0	1	-	-	-	-
0	0	1	0	-	-	-	-
0	0	1	1	-	-	-	-
0	1	0	0	0	1	0	0
0	1	0	1	0	0	1	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	-	-	-	-
1	1	0	1	-	-	-	-
1	1	1	0	-	-	-	-
1	1	1	1	1	0	0	1

(a) $w = \sum(8, 15)$

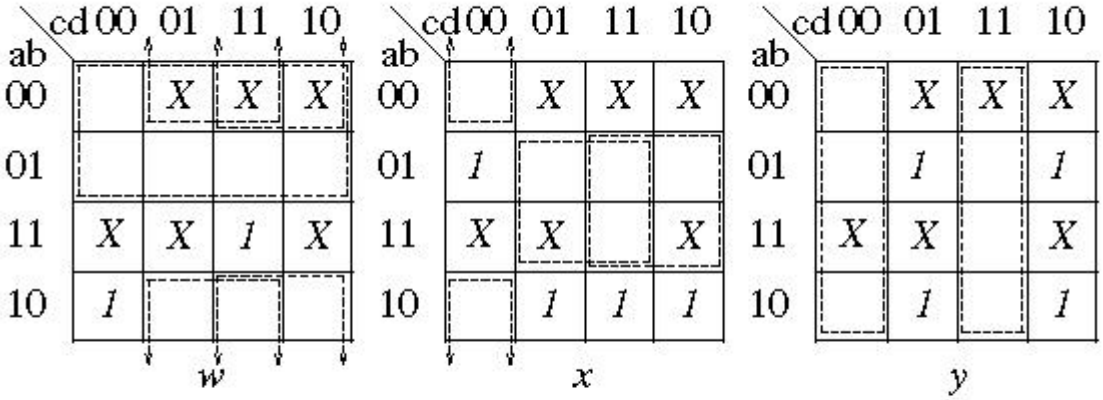
$x = \sum(4, 9, 10, 11)$

$y = \sum(5, 6, 9, 10)$

$z = d$



(b) The sum-of-product equations were developed in Assignment3.



$$w = ab + ac'd' \qquad w' = a' + b'd + b'c$$

$$x = b'c + b'd' + bc'd' \qquad x' = bd + a'c'd + bc$$

$$y = cd' + c'd \qquad y' = c'd' + cd$$

		$abcd$	wxy
a'	(1)	0 - - -	1 - -
$b'd$	(2)	- 0 - 1	1 1 -
$b'c$	(3)	- 0 1 -	1 1 -
$bc'd'$	(4)	- 1 0 0	- 1 -
cd'	(5)	- 1 0 -	- - 1
$c'd$	(6)	- 0 1 -	- - 1
			CTT

(c) A four bit binary adder chip can be used to subtract the -2-1 bits from the 84 bits, i.e,

$$wxyz = ab00 - 00cd = ab00 + (1111 - 00cd + 1)$$

$$= ab00 + 11c'd' + 1$$

$$= ab01 + 11c'd'$$