ECE-223, Assignment #6

Digital Design, M. Mano, 3rd Edition, Chapter 5

- 5.2) Construct a JK flip-flop using a D Flip-flop, a 2-to-1 line multiplexer and an inverter.
- 5.4) A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.
 - a) Tabulate the characteristic table.
 - b) Derive the characteristic equation.
 - c) Tabulate the excitation table.
 - d) Show how the PN flip-flop can be converted to a D flip-flop.
- 5.6) A sequential circuit with two D Flip-Flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations:

$$A(t+1) = x'y + xA$$
$$B(t+1) = x'B + xA$$
$$z = B$$

- a) Draw the logic diagram of the circuit.
- b) List the state table for the sequential circuit.
- c) Draw the corresponding state diagram.
- 5.12) Reduce the number of states in the following state table and tabulate the reduced state table.

Present	Next State		Output	
State	x =0	x = 1	x =0	x = 1
a	f	b	0	0
b	d	c	0	0
С	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

- 5-16) Design a sequential circuit wit twp D Flip-Flops, A and B, and one input x. When x = 0, then the state of the circuit remains the same. When x = 1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.
- 5-17) Design a one input, one output serial 2's complimenter. The circuit accepts a string of bits from the input and generates the 2's compliment at the output. The circuit can be reset asynchronously to start and end the operation.
- 5-19) A sequential circuit has three flip-flops A, B, C; one input x; and one output, y. The state diagram is shown in Fig.P5-19. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.
 - a) Use D flip-flops in the design
 - b) Use J-K flip-flops in the design

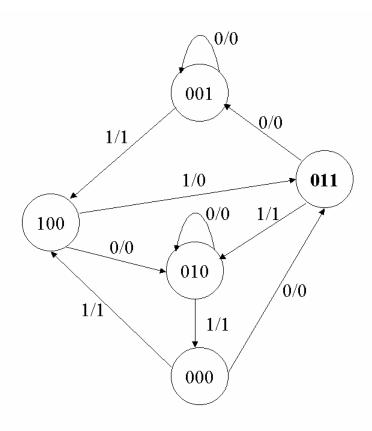


Fig.P5-19

5-20) Design the sequential circuit specified by the state diagram of Fig. 5-19 using T flip-flops.

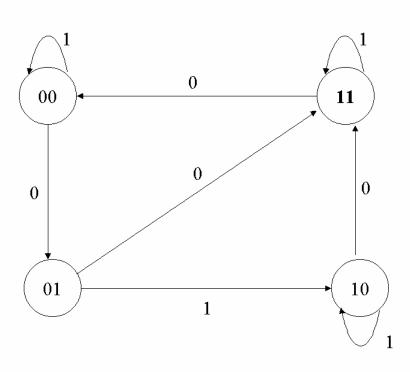


Fig. 5-19