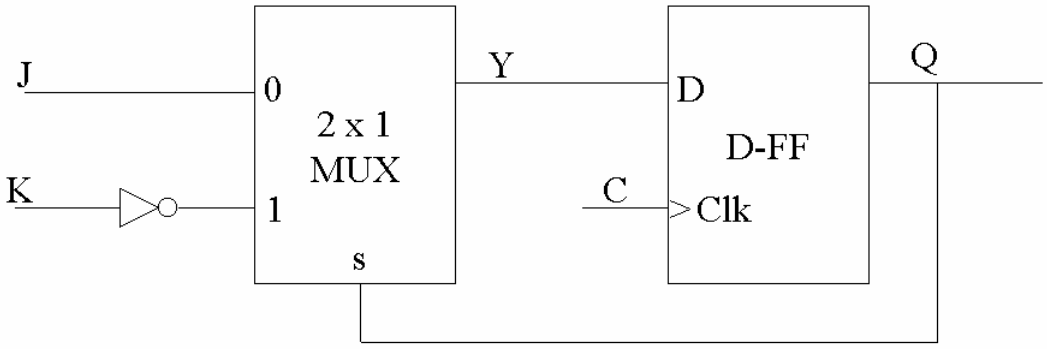
ECE-223, Solutions for Assignment #6

Digital Design, M. Mano, 3rd Edition, Chapter 5

5.2) Construct a JK flip-flop using a D Flip-flop, a 2-to-1 line multiplexer and an inverter.



5.4) A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

a) Tabulate the characteristic table.
b) Derive the characteristic equation.
c) Tabulate the excitation table.
d) Show how the PN flip-flop can be converted to a D flip-flop.

a)

P	N	Q(t+1)
0	0	0
0	1	Q(t)
1	0	Q′(t)
1	1	1

b)

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

N

P\NQ	00	01	11	10
0	0	0	1	0
1	1	0	1	1

P

$Q(t+1) = PQ' + NQ$

c)

Q(t)	Q(t+1)	P	N
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

d) By connecting P and N together.

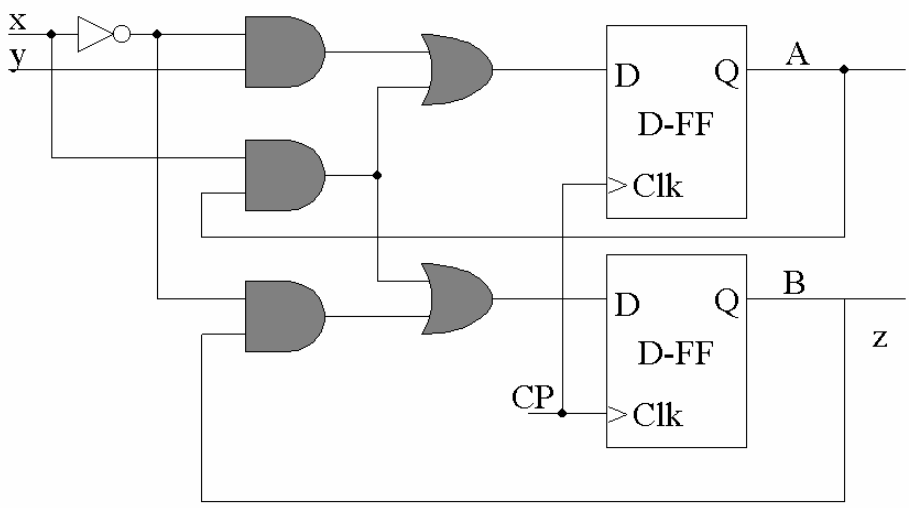
$Q(t+1) = DQ' + DQ = D$

5.6) A sequential circuit with two D Flip-Flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations:

$A(t+1) = x'y + xA$
$B(t+1) = x'B + xA$
$z = B$

a) Draw the logic diagram of the circuit.
b) List the state table for the sequential circuit.
c) Draw the corresponding state diagram.

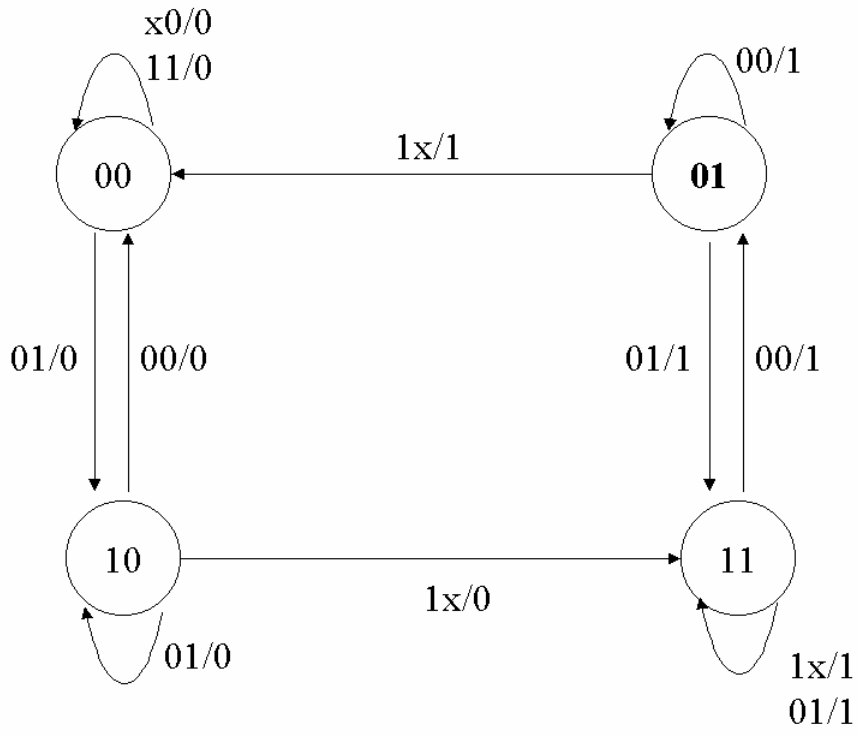
a)



b)

Present State		Inputs		Next State		Output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

c)



5.12) Reduce the number of states in the following state table and tabulate the reduced state table.

Present State	Next State		Output	
	x =0	x =1	x =0	x =1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

Present State	Next State		Output	
	x =0	x =1	x =0	x =1
a	f	b	0	0
b	d	a	0	0
d	g	a	1	0
f	f	b	1	1
g	g	d	0	1

5-16) Design a sequential circuit with two D Flip-Flops, A and B, and one input x.
When x = 0, then the state of the circuit remains the same. When x =1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

Present State AB	Input x	Nest State AB
00	0	00
00	1	01
01	0	01
01	1	11
10	0	10
10	1	00
11	0	11
11	1	10

B

A\Bx	00	01	11	10
0	0	0	1	0
1	1	0	1	1

A

$D_A = AX' + BX$

B

A\Bx	00	01	11	10
0	0	1	1	1
1	0	0	0	1

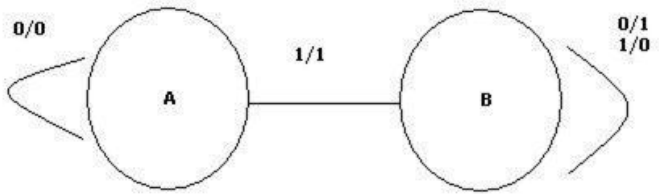
A

$D_B = A'X + BX'$

5-17) Design a one input, one output serial 2's complimenter. The circuit accepts a string of bits from the input and generates the 2's compliment at the output. The circuit can be reset asynchronously to start and end the operation.

Solution:

The output is 0 for all 0 inputs until the first 1 occurs at which time, the output is 1. Thereafter, the output is the complement of the input.



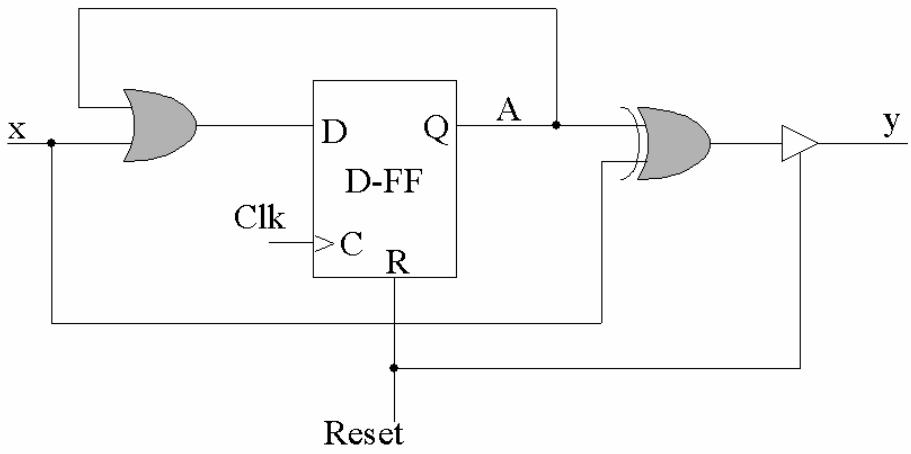
A: starting state

The state diagram has two states

State 0 : Output = Input
State1 : Output = Complement of input

PS A	Inp. x	NS A	Out y
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	0

$D_A = A + x$
$y = A \oplus x$



5-19) A sequential circuit has three flip-flops A, B, C; one input x; and one output, y. The state diagram is shown in Fig.P5-19. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.

a) Use D flip-flops in the design
b) Use J-K flip-flops in the design

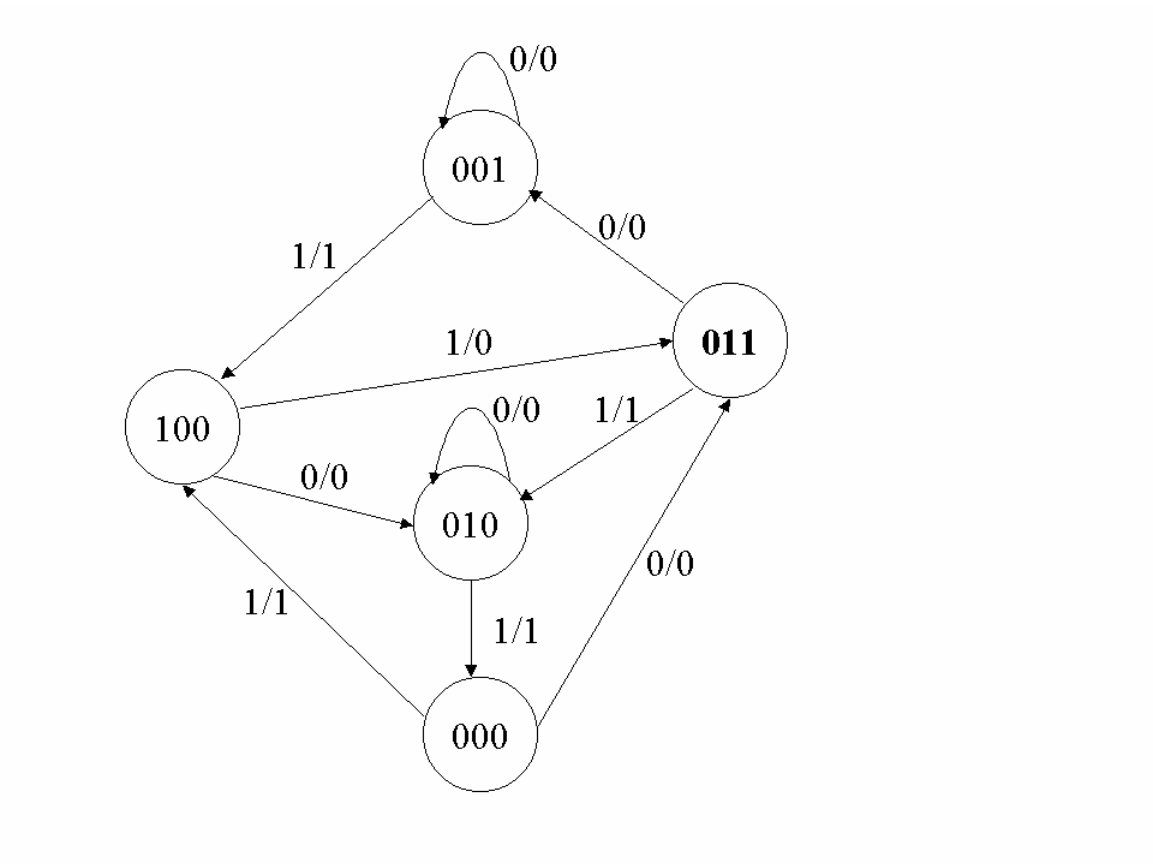
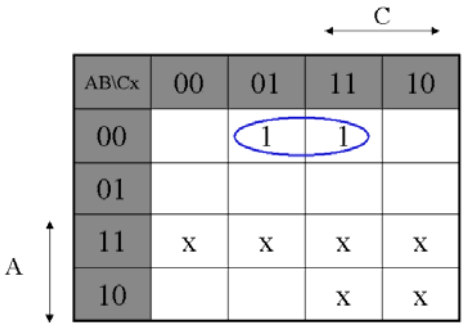


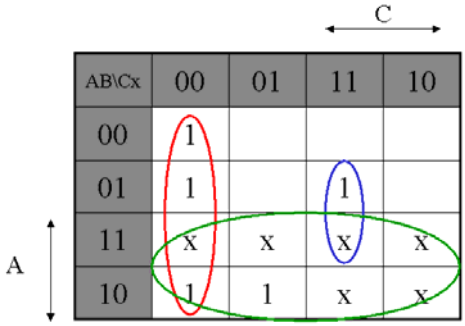
Fig.P5-19

a)

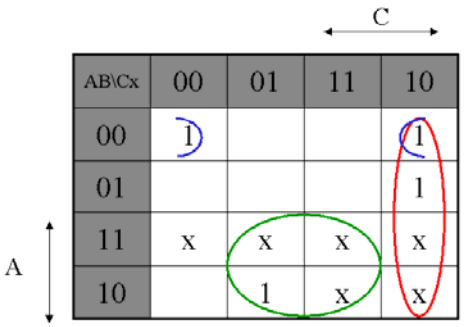
Present State			Input	Next State			Output
A	B	C	x	A	B	C	y
0	0	0	0	0	1	1	0
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	1
1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	0



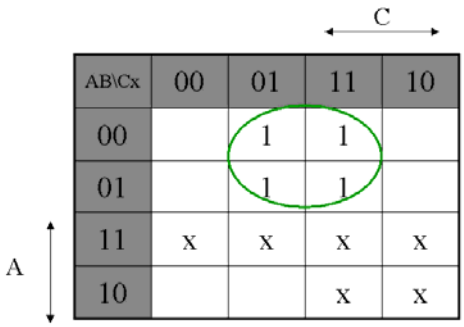
$D_A = A'B'X$



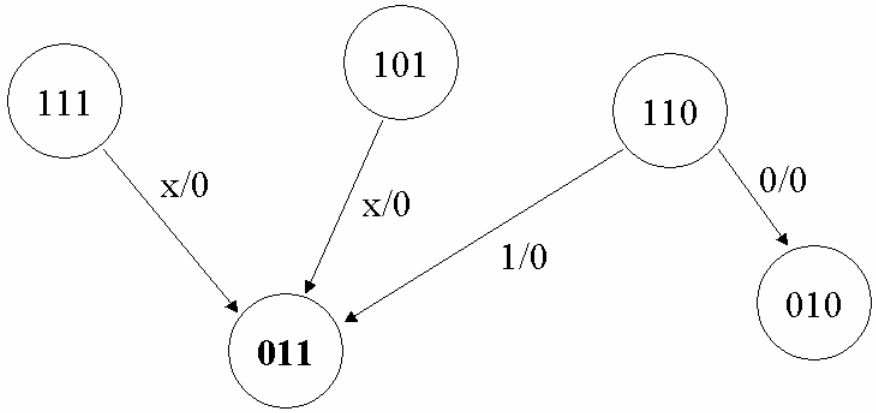
$D_B = A + C'x' + BCx$



$D_C = Ax + Cx' + A'B'x'$



$D_D = A'x$



b) Use JK flip-flops:

J_A	K_A	J_B	K_B	J_C	K_C
0	X	1	X	1	X
1	X	0	X	0	X
0	X	0	X	X	0
1	X	0	X	X	1
0	X	X	0	0	X
0	X	X	1	0	X
0	X	X	1	X	0
0	X	X	0	X	1
X	1	1	X	0	X
X	1	1	X	1	X

$J_A = B'x$ $J_B = A + C'x'$ $J_C = Ax + A'B'x'$
$K_A = 1$ $K_B = C'x + Cx'$ $K_C = x$

Self-correction because $K_A = 1$

5-20) Design the sequential circuit specified by the state diagram of Fig. 5-19 using T flip-flops.

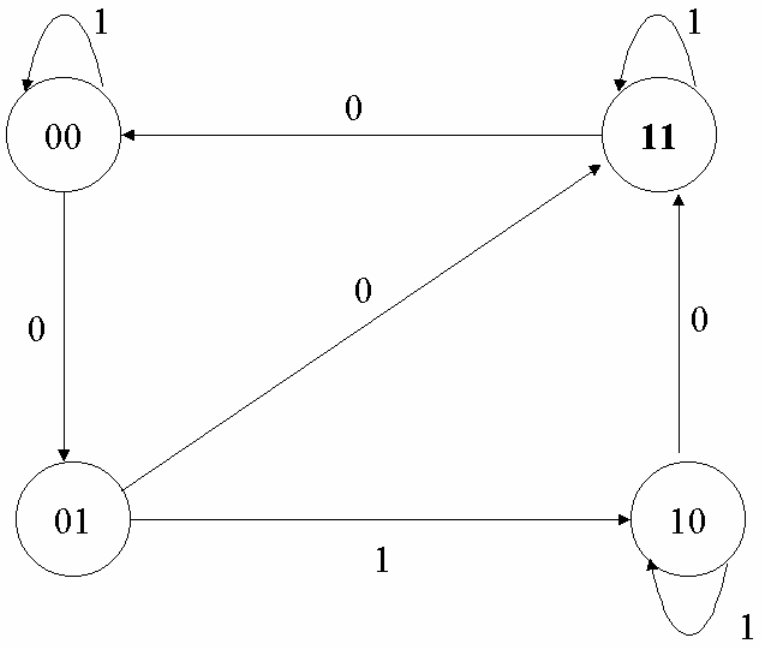


Fig. 5-19

From State table (Table 5-4 from Digital Design, M. Mano, 3rd Edition, pp.186)

$T_A (A, B, x) = \sum (2, 3, 6)$
$T_B (A, B, x) = \sum (0, 3, 4, 6)$

B

A\Bx	00	01	11	10
0	1		1	
1	1			1

A

$T_B = A'B+Bx'$

B

A\Bx	00	01	11	10
0			1	1
1				1

A

$T_A = Ax'+B'x'+A'Bx$