ECE-223, Assignment #7

Digital Design, M. Mano, 3rd Edition, Chapter 6

6.6) Design a 4-bit shift register with parallel load using *D flip-flops.* These are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data is transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register dose not change.

6.7) Draw the logic diagram of a 4-bit register with four *D flip-flops* and 4×1 mutiplexers with mode selection input s_1 and s_0. The register operates according to the following function table:

s_1	s_0	Register Operation
0	0	No Change
0	1	Complement the four Output
1	0	Clear register to 0 (Synch)
1	1	Load parallel data

6-9) Two ways for implementing a serial adder (A+B) is shown in Section 6-2. It is necessary to modify the circuits to convert them to serial subtractors (A-B).
  a) Using the circuit of Fig. 6-5, show the changes needed to perform A + 2's complement of B.
  b) Using the circuit of Fig. 6-6, show the changes needed by modifying Table 6-2 from an adder to a subtractor circuit. (See Problem 4-12).

6-10) Design a serial 2's complementer with shift register and a flip-flop. The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.

6-13) Show that a BCD ripple counter can be constructed using a 4-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.

6-24) Design a counter with *T flip-flops* that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Show that when binary states 010 and 101 are considered as *don't care* conditions, the counter may not operate properly. Find a way to correct the design.