ECE 223
Digital Circuits and Systems

Introduction

M. Sachdev,

Dept. of Electrical & Computer Engineering

University of Waterloo

University of **Waterloo**

Course Information - People

- **Instructor**
  - Manoj Sachdev; msachdev@uwaterloo.ca; CEIT 4015

- **Lab Technologist**
  - Eric Praetzel, praetzel@ece.uwaterloo.ca; E2 - 2357

- Teaching Assistants
  - David Li   x37434
  - S.M. Jahinuzzaman   x32033
  - Salmaz Ghaznavi   x37792

Course Information - Text

- Text Book – M. Morris Mano, Digital Design, 3rd Edition, Printice Hall
  - Lecture Notes http://ece.uwaterloo.ca/~msachdev
- Laboratory manual
  - Download from http://ece.uwaterloo.ca/~ece223
- Lectures
  - Tue, Wed, Fri 9.30 – 10.20 am; RCH 302
  - Tutorials
    - (i) Tue @10.30-11.20 HH280;
    - (ii) Thurs @9.30-10.20 ML349;
    - (iii) Thurs @11.30-12.20 DWE3516

Course Information - Labs

- Lab0 & 1 – Individually; Lab2 & 3 – group of 2
- Marking Scheme
  - Final exam marks >50%
    - -- Labs 30%; Midterm 20%; Final 50%
  - Final exam marks <50%
    - -- Labs 0%, Midterm 20%, Final 50%

Coverage of Topics

- **Introduction [1]**
  - □ This Lecture
- **Number Systems [2]**
  - □ Radix, radix conversion, complements, subtraction, number representation, codes
- **Boolean Algebra, Logic Gates & Simplification [8]**
  - □ Theorems, functions, canonical & standard forms, Digital logic gates, Logic simplification – Karnaugh map, sum of products, product of sums, don't cares

Coverage of Topics ..

- **Combinational Logic Design [8]**
  - □ Analysis procedure, Design procedure, Adders, Subtractors, Decoders, Encoders, etc.
- **Sync. Seq. Logic, Registers, Counters [8]**
  - □ Latches and flip-flops, Analysis, State reduction, Design procedure, Registers, Ripple counters, Synchronous counters
- **Memory & Programmable Logic [3]**
  - □ RAM, ROM, PLA, PAL, FPGAs

Coverage of Topics ..

- Asynchronous Sequential Logic
  - Analysis procedure, Circuits with latches, Design pocedure, State reduction and Flow Table, Race-free state assignment, Hazards

Relationship with Future Courses

- ECE223 provides the foundation for higher order digital systems & digital integrated circuit courses
  - ECE222 – Digital computers
  - ECE324 – Microprocessor Systems & Interfacing
  - ECE427 – Digital Systems Engineering
  - ECE438 – Digital Integrated Circuits
  - ECE437 – Integrated VLSI Systems

Schedule (tentative)

Week	Dates	Tutorial	Lab
1	Sept 10 - 14	-	-
2	17 - 21	Ass #1	Lab0
3	24 - 28	Lab 1 Intro	Lab0
4	Oct. 1 - 5	Ass #2	Lab1
5	8 - 12	Ass #3	Lab1
6	15 - 19	Midterm Review	
7	22- 26	Ass #4/Lab 2 Intro	
8	29 – Nov. 2	Ass #5	Lab2
9	Nov. 5 - 9	Ass #6	Lab2
10	12 - 16	Lab3 Intro	
11	19 - 23	Ass #7	Lab3
12	26 -30	Ass #8	Lab3
13	Dec. 3 - 7		