ECE 223
Digital Circuits and Systems

Registers & Counters

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Registers

- Register is a group of flip-flops
  - *n*-bit register has *n* flip-flops
  - Can hold *n* bits of binary data
  - Register may also contain combinational logic

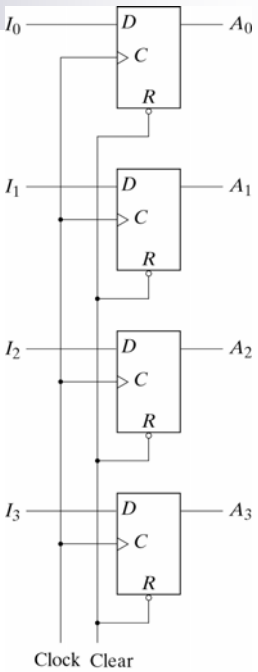


Fig. 6-1 4-Bit Register

Register with Parallel Load

- Specific control signal to load n-bit data
  - Load =0, register retains the data
  - Load = 1, register accepts new data

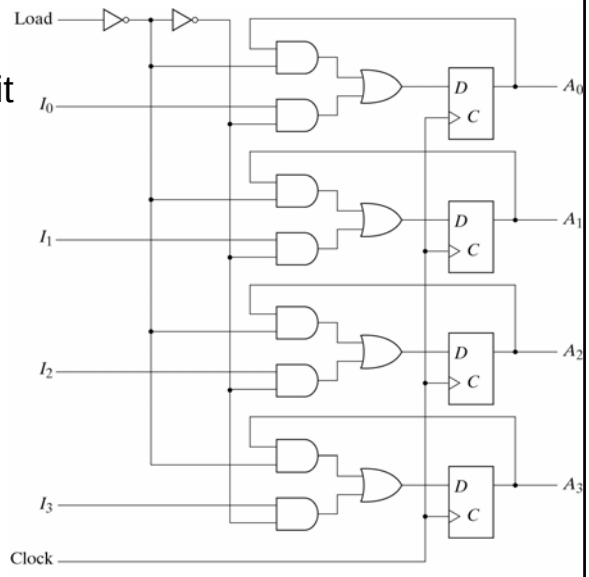


Fig. 6-2 4-Bit Register with Parallel Load

Shift Register

- Capable of shifting data in one or both directions
  - Clock controls the shift operation
- Figure shows a simple shift register with left to right data shifting capability

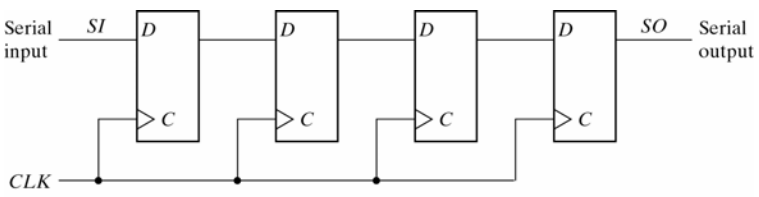


Fig. 6-3 4-Bit Shift Register

4

Serial Data Transfer

- Serial mode → Data is transferred one bit at a time

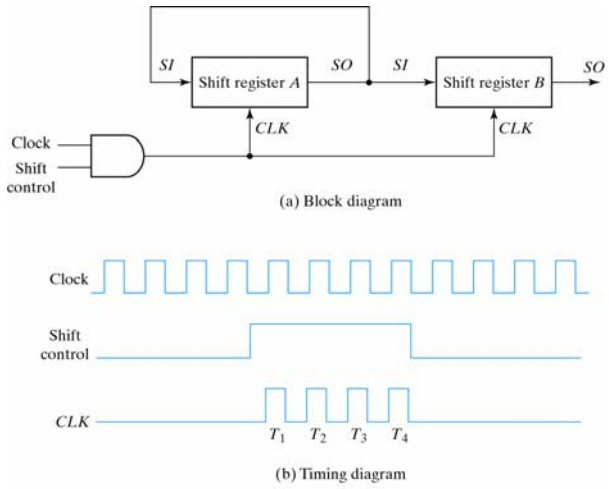


Fig. 6-4 Serial Transfer from Register *A* to register *B*

Serial Addition

- Parallel adders
  - Faster,
  - cost more logic
- Serial adders
  - Slower
  - n-bit addition → n clock cycles
  - Less hardware

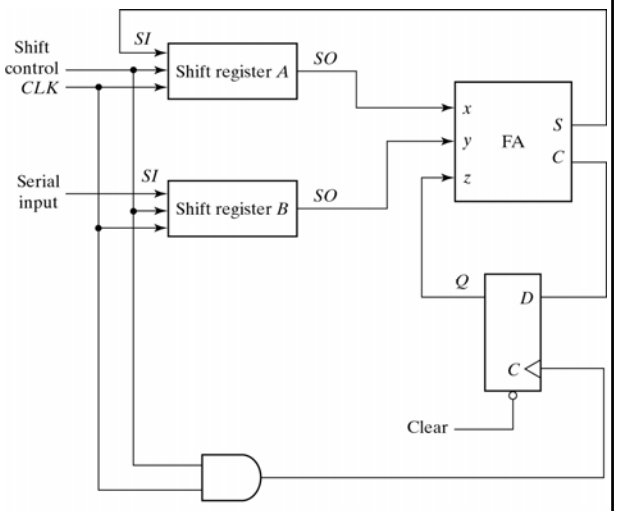


Fig. 6-5 Serial Adder

Universal Shift Register

Mode Control		Operation
S1	S0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Para load

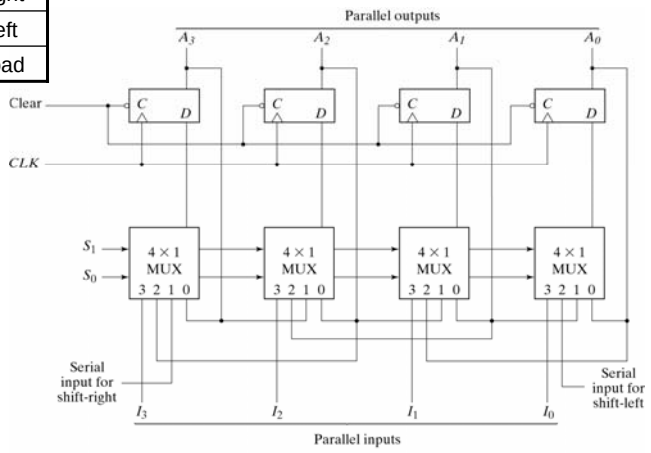


Fig. 6-7 4-Bit Universal Shift Register

Ripple (Asynchronous) Counter

- Counts the binary sequence
  - Negative edge triggered
  - Output of one flip-flop → Clock to the next
  - Clock skew adds up

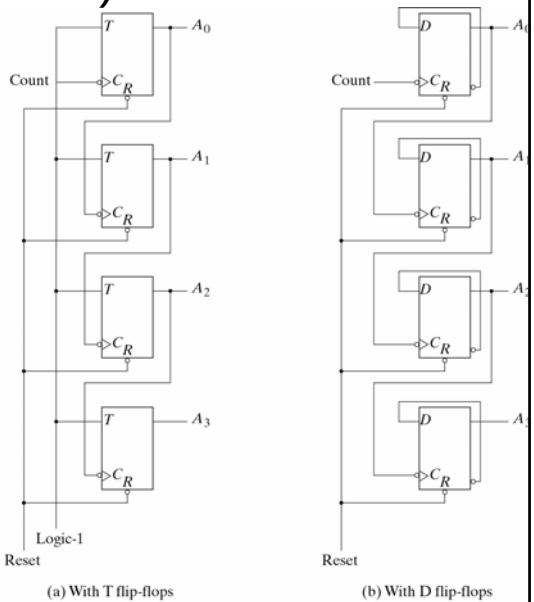


Fig. 6-8 4-Bit Binary Ripple Counter

BCD Ripple Counter

- Counter must reset itself after counting the terminal count

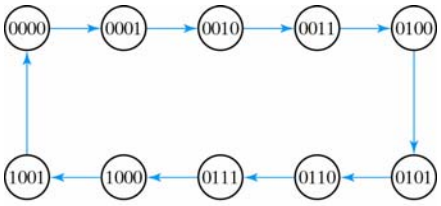


Fig. 6-9 State Diagram of a Decimal BCD-Counter

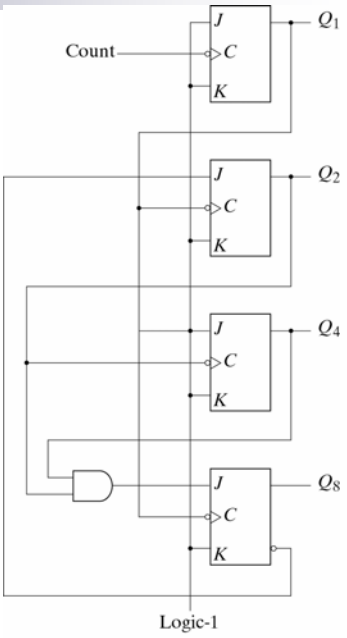


Fig. 6-10 BCD Ripple Counter

9

Synchronous Counters

- A common clock is applied to all flip-flops
  - Clock skew does not add up
  - Faster than ripple counters
- Synchronous counters can be designed using **sequential circuit procedure**
- Synchronous binary counter

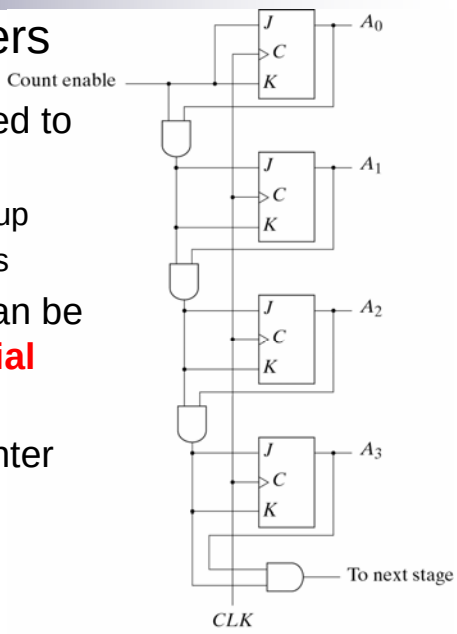


Fig. 6-12 4-Bit Synchronous Binary Counter

Up-Down Binary Counter

- Can count up (0000 → 1111) or down (1111 → 0000) binary sequence

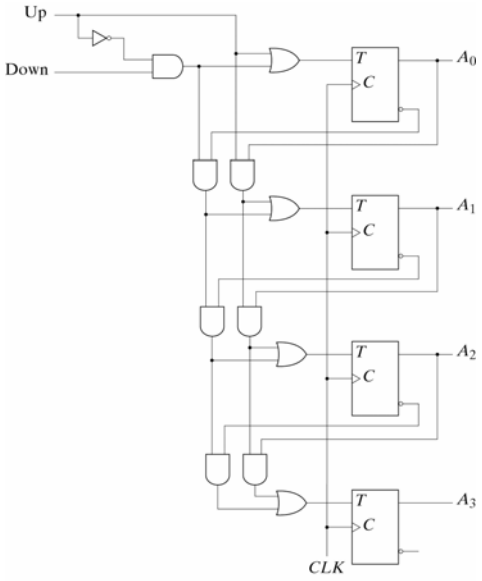


Fig. 6-13 4-Bit Up-Down Binary Counter

11

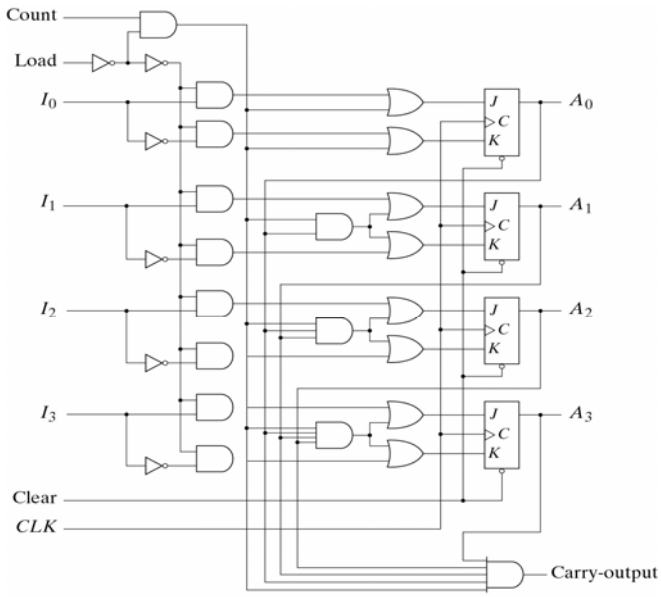
Synchronous BCD Counter

- Design a synchronous BCD counter with T flip-flops

Present State				Next State				Out	Flip-flop inputs			
Q8	Q4	Q2	Q1	Q8	Q4	Q2	Q1	y	TQ8	TQ4	TQ2	TQ1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

12

Binary Counter with Parallel Load



13

BCD Counter & Modulo-N Counter

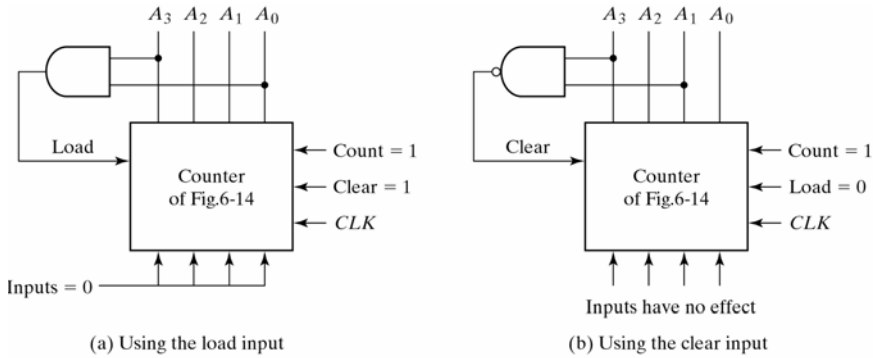


Fig. 6-15 Two ways to Achieve a BCD Counter Using a Counter with Parallel Load

- *Home work - Suppose we want to design a counter with 1,2,3,4,5,6,7,8,9 sequence (mod-9 counter)?*

14

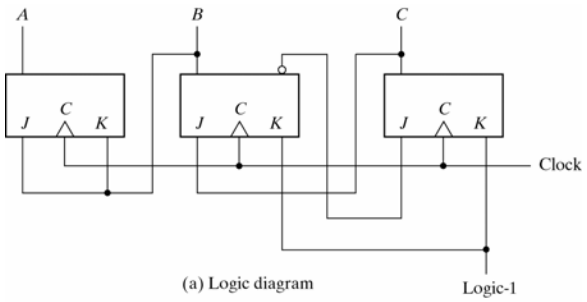
Counter with Unused States

- A circuit with *n* flip-flops has 2^n states
  - We may have to design a counter with a given sequence (unused states)
  - Unused states may be treated as don't care or assigned specific next state
  - Outside noise may cause the counter to enter unused state
    - Must ensure counter eventually goes to the valid state

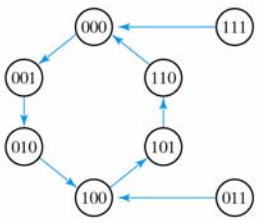
Present State			Next State			Flip-flop Inputs					
A	B	C	A	B	C	JA	KA	JB	KB	JC	KC
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

15

Counter with Unused States



(a) Logic diagram

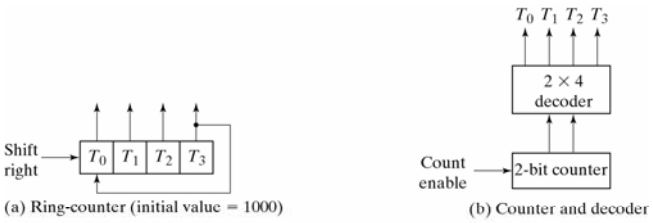


(b) State diagram

Fig. 6-16 Counter with Unused States

16

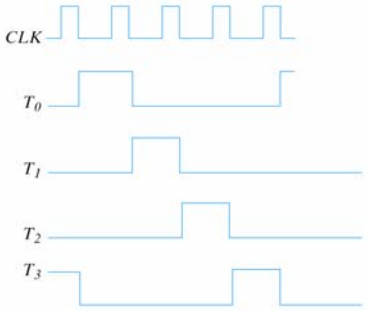
Ring Counter



(a) Ring-counter (initial value = 1000)

(b) Counter and decoder

Capable of generating different timing signals



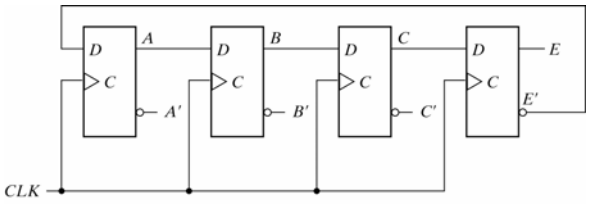
(c) Sequence of four timing signals

Fig. 6-17 Generation of Timing Signals

17

Johnson Counter

- Number of states of a ring counter can be doubled



(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs A	B	C	E	AND gate required for output
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

Fig. 6-18 Construction of a Johnson Counter

18

Book Sections – Registers & Counters

- Material is covered in Sections 6.1 – 6.5

19