University of Waterloo
Department of Electrical & Computer Engineering
E&CE 223 Digital Circuits and Systems

Solution for Final Examination
April 5, 2004

Total Time = 3 hours, Total Marks = 100

Student Name:			**Student ID:**	
1.	**2.**	**3.**	**4.**	**5.**
6.	**7.**	**8.**	**9.**	**Total**

Attempt all problems. Show all work. If information appears to be missing make a reasonable assumption, state it, and proceed. Calculators are not needed and are not allowed.

Problem 1 [10 Marks]

A) What is noise margin in digital logic gates? Explain briefly. **[2]**

Noise margin is the minimum external noise voltage that causes an undesirable change in the circuit output.

B) A smart engineer designed a 3 input NOR gate with **negative logic**, however he/she has trouble devising its truth table. You are expected to help him/her realize the truth table. **[4]**

Inputs ABC	Output Z
000	1
001	1
010	1
011	1
100	1
101	1
110	1
111	0

C) What is a race condition in asynchronous sequential circuits? Give an example of non-critical race condition. **[2+2]**

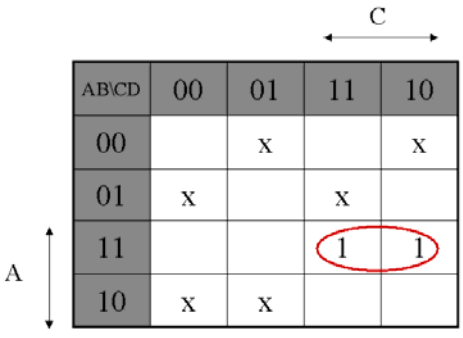
A race condition is said to exist in an asynchronous sequential circuit when two or more binary state variable change value in response to a change in an input variable.

If the final stable state that the circuit reaches dose not depend on the order in which the state variable change, the race is called a non-critical race.

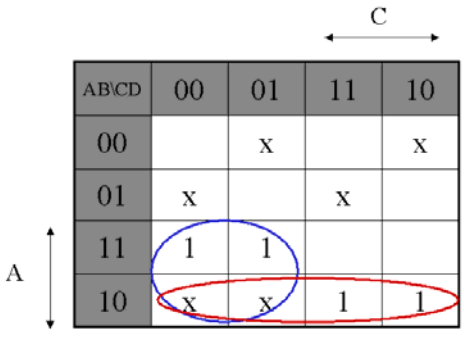
Problem 2 [12 marks]

A design engineer devised a new code, *Mycode*, to represent the decimal numbers. You are required to design a combinational circuit that converts a number represented in *Mycode* to BCD**.**

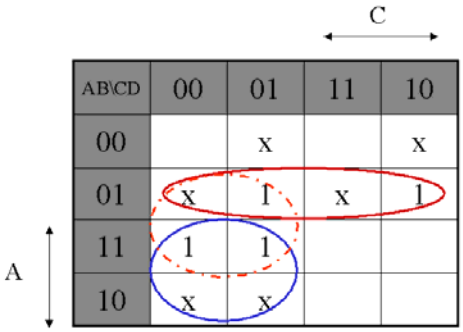
Decimal number	*Mycode* ABCD	BCD # EFGH
0	0000	0000
1	0011	0001
2	0101	0010
3	0110	0011
4	1010	0100
5	1011	0101
6	1100	0110
7	1101	0111
8	1110	1000
9	1111	1001



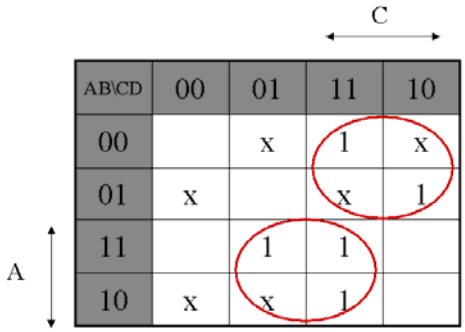
E = ABC



F = AC′ + AB′



G = AC′ + A′B
G = BC′ + A′B



H = AD + A′C

Problem 3 [12 marks]

A) For a carry look-ahead adder, redefine the carry propagate and carry generate as follow:

$P_i = A_i + B_i$; *and* $G_i = A_iB_i$

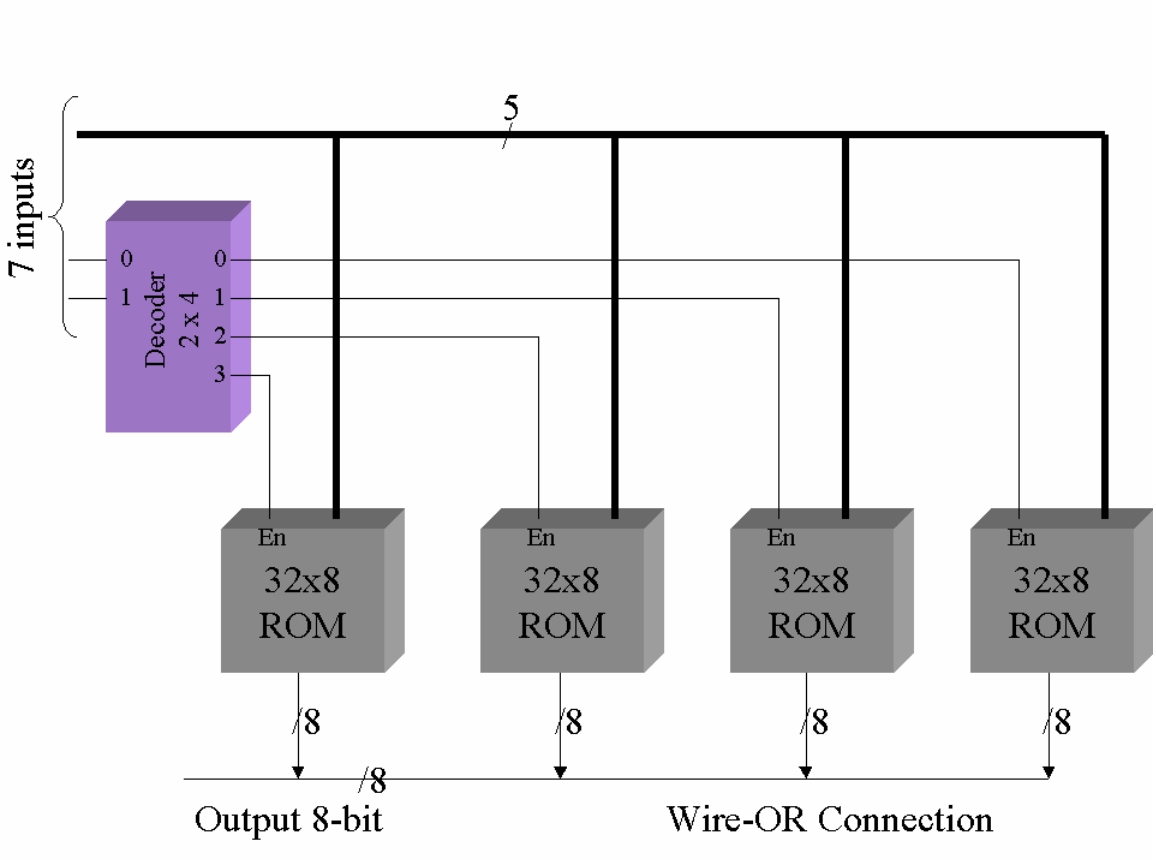
Show that the output carry and the sum of a full adder becomes

$C_{i+1} = (C'_iG'_i + P'_i)' = G_i + P_iC_i$; and $S_i = (P_iG'_i)C'_i + (PiGi)'C_i$. **[6]**

$(C_i' G_i' + P_i')' = (C_i + G_i). P_i$
$= C_i P_i + G_i P_i$
$= A_i B_i (A_i + B_i) + P_i C_i$
$= A_i B_i + P_i C_i$
$= G_i + P_i C_i$
$= A_i B_i + (A_i + B_i)C_i$
$= A_i B_i + A_i C_i + B_i C_i = C_{i+1}$

$(P_iG_i') \oplus C_i = (A_i + B_i) (A_i B_i)' \oplus C_i$
$= (A_i + B_i) (A_i' + B_i') \oplus C_i$
$= (A_i' B_i + A_i B_i') \oplus C_i$
$= A_i \oplus B_i \oplus C_i = S_i$

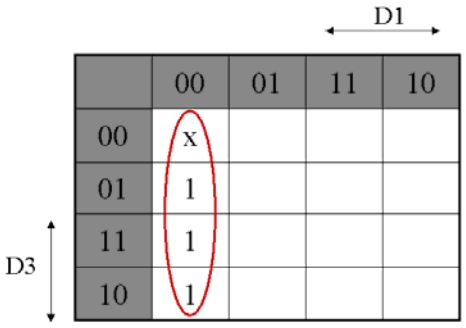
B) Given a 32x8 ROM chip with an enable input, show the block level required connections to construct a 128x8 ROM with 4 ROM chips and a decoder. **[6]**



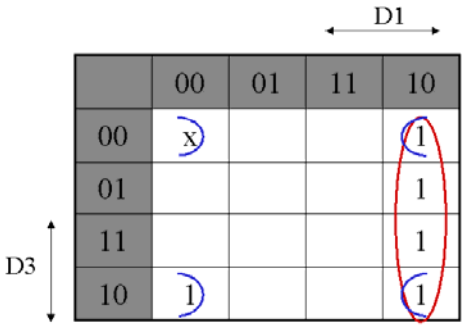
Problem 4 [10 marks]

Design a 4-input priority encoder with inputs and outputs as described in the table below. Please note that the input *D0* has highest priority and *D3* has lowest priority.

Inputs				**Outputs**		
D3	***D2***	***D1***	***D0***	***X***	***Y***	***V***
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	0
X	X	X	1	1	1	1



$x = D_0' D_1'$

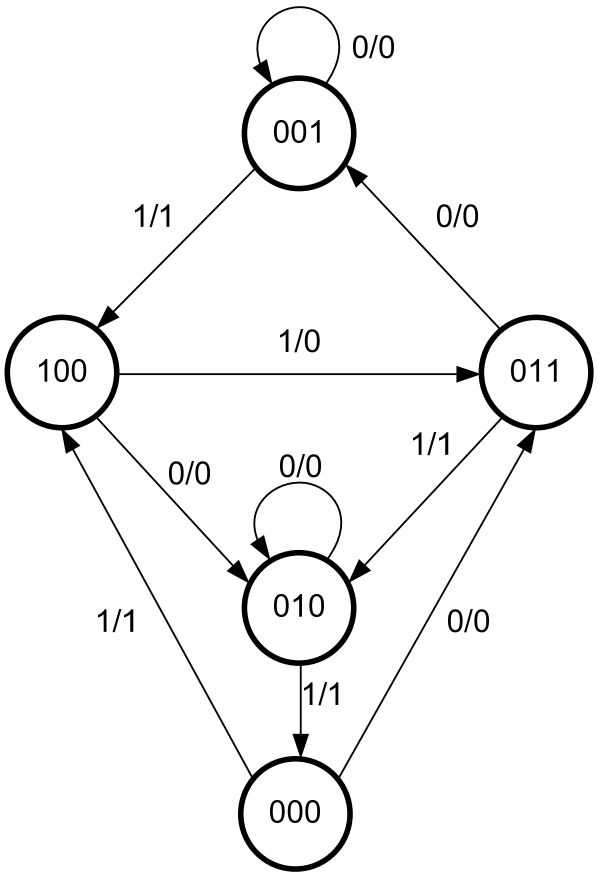


$y = D_0' D_1 + D_0' D_2'$

$V = D_0 + D_1 + D_2 + D_3$

Problem 5 [16 marks]

A sequential circuit has three flip-flops, *A, B, C*; one input *x*, and one output, *y*. The state diagram is shown below. The circuit is designed by treating the unused states as don't care conditions. The final circuit must be analyzed to ensure that it is self-correcting (i.e., if the circuit enters in any of the unused states, after finite number of clock cycles it comes to a used state.). Use *JK* flip-flops for the design.



Present State			Input	Next State			Output
A	B	C	x	A	B	C	y
0	0	0	0	0	1	1	0
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	1
1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	0

J_A	K_A	J_B	K_B	J_C	K_C
0	X	1	X	1	X
1	X	0	X	0	X
0	X	0	X	X	0
1	X	0	X	X	1
0	X	X	0	0	X
0	X	X	1	0	X
0	X	X	1	X	0
0	X	X	0	X	1
X	1	1	X	0	X
X	1	1	X	1	X

$J_A = B'x$ $J_B = A + C'x'$ $J_C = Ax + A'B'x'$

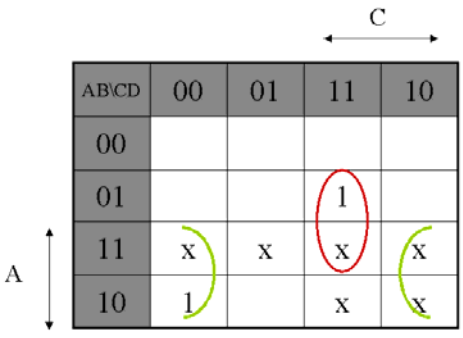
$K_A = 1$ $K_B = C'x + Cx'$ $K_C = x$

Self-correction because $K_A = 1$

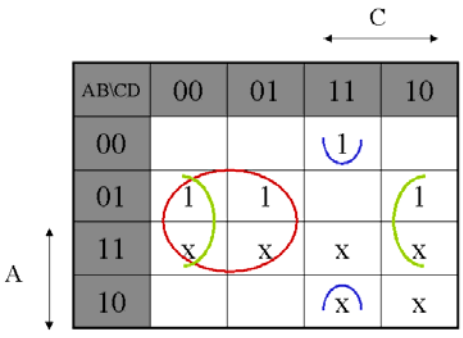
Problem 6 [14 marks]
Design a synchronous BCD counter with *Data* flip-flops.

Present State				Next State			
A	B	C	D	A	B	C	D
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

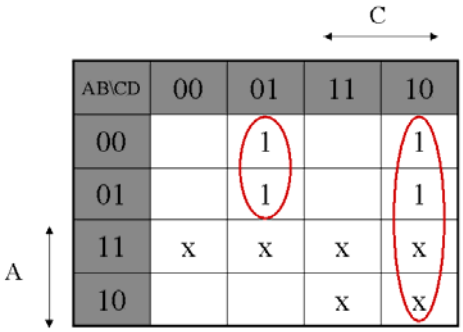
d(A,B,C,D) = ∑ (10,11,12,13,14,15)



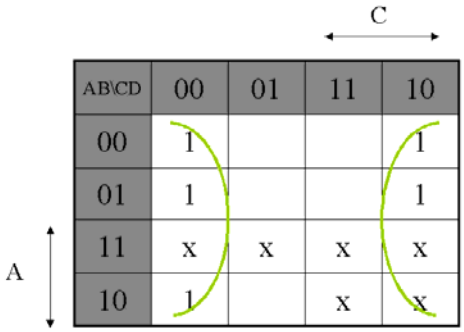
$D_A = AD' + BCD$



$D_B = BC' + BD' + B'CD$

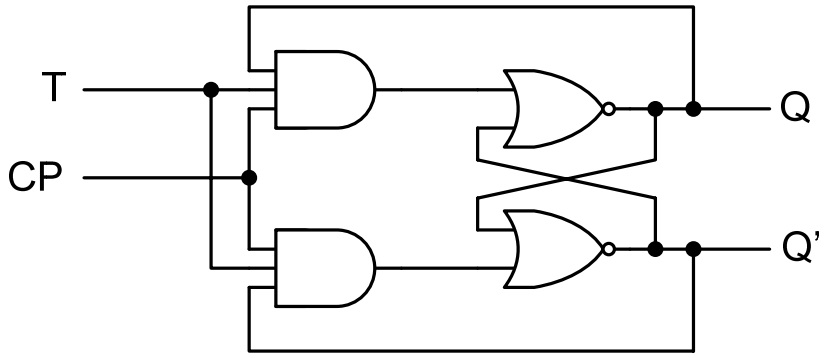

C
A
AB\CD
00
01
11
10
00
1
1
01
1
1
11
x
x
x
x
10
x
x

$D_C = CD' + A'C'D$


C
A
AB\CD
00
01
11
10
00
1
1
01
1
1
11
x
x
x
x
10
1
x
x

$D_D = D'$

Problem 7 [10 marks]
Analyze a given toggle flip-flop as shown below as an asynchronous sequential circuit. Obtain the transition table and show that the circuit is unstable when both T and CP are equal to 1.



Let CP = C , Q = Y

S = TCy′ R = TCy

Y = S + R′y
= TCy′ + (TCy)′ y
= TCy′ + Ty′ + C′y

T

y\TC	00	01	11	10
0	0	0	1	0
1	1	1	0	1

y

➔ when T =1 and C = 1 then Y ≠ y ➔ circuit is unstable.

Problem 8 [16 marks]

The state table of an asynchronous circuit with three SR latches is shown below. Reduce the number of states in the state table using implication table.

Present State ABC	Input x	Next State ABC	Flip-flop Inputs SA RA SB RB SC RC	Output Y
001	0	001	0 X 0 X X 0	0
001	1	010	0 X 1 0 0 1	0
010	0	011	0 X X 0 1 0	0
010	1	100	1 0 0 1 0 X	**1**
011	0	001	0 X 0 1 X 0	0
011	1	**010**	**0 X X 0 0 X**	0
100	0	101	X 0 0 X 1 0	0
100	1	100	X 0 0 X 0 X	1
101	0	001	0 1 0 X X 0	0
101	1	100	X 0 0 X 0 1	1

State\Input	x = 0	x = 1
a (001)	a,0	b,0
b (010)	c,0	d,1
c (011)	a,0	b,0
d (100)	e,0	d,1
e (101)	a,0	d,1

b	✗			
c	✓	✗		
d	✗	c,e✗	✗	
e	✗	a,c✓	✗	a,e✗
	a	b	c	d

(a,c) , (e,b), (d)