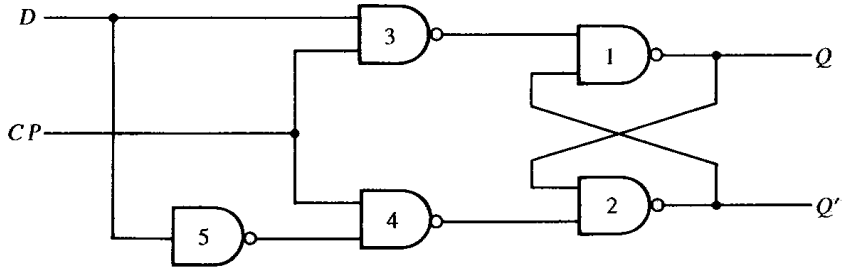
Problem Set 6

6-1 Construct a *D* flip-flop that has the same characteristics as the one shown in Fig. 6-5, but instead of using NAND gates, use NOR and AND gates. (Remember that a one-input NOR gate is equivalent to an inverter.)

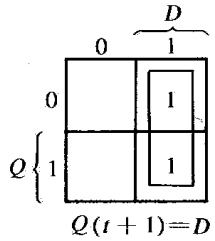
6-2 Construct a *D* flip-flop that has the same characteristics as the one shown in Fig. 6-5, but instead of using NAND gates, use NOR gates.



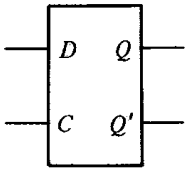
(a) Logic diagram

Q	D	Q(t + 1)
0	0	0
0	1	1
1	0	0
1	1	1

(b) Characteristic table



(c) Characteristic equation



(d) Graphic symbol

FIGURE 6-5
D flip-flop

6-4 Draw the logic diagram of a master–slave *D* flip-flop. Use NAND gates.

6-9 Derive the state table and the state diagram of the sequential circuit shown in Fig. P6-9. Explain the function that the circuit performs.

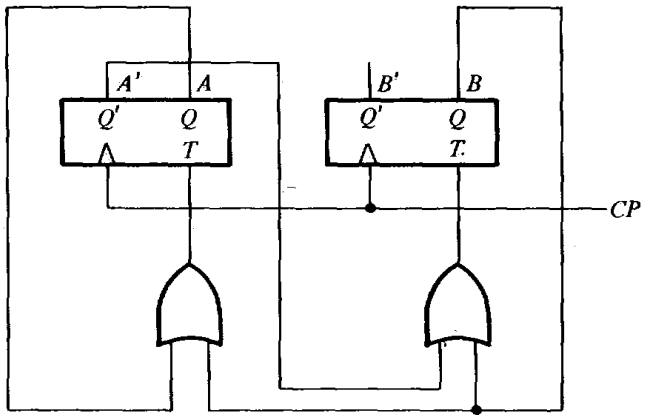


FIGURE P6-9

6-12 A sequential circuit has two *JK* flip-flops, *A* and *B*; two inputs, *x* and *y*; and one output, *z*. The flip-flop input functions and the circuit output function are as follows:

$$JA = Bx + B'y' \qquad KA = B'xy'$$

$$JB = A'x \qquad KB = A + xy'$$

$$z = Axy + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c) Derive the next-state equations for *A* and *B*.

6-21 Design a sequential circuit with two *JK* flip-flops, *A* and *B*, and two inputs, *E* and *x*. If $E = 0$, the circuit remains in the same state regardless of the value of *x*. When $E = 1$ and $x = 1$, the circuit goes through the state transitions from 00 to 01 to 10 to 11 back to 00, and repeats. When $E = 1$ and $x = 0$, the circuit goes through the state transitions from 00 to 11 to 10 to 01 back to 00, and repeats.

6-22 A sequential circuit has three flip-flops, A, B, C; one input, x; and one output, y. The state diagram is shown in Fig. P6-22. The circuit is to be designed by treating the unused states as don't-care conditions. The final circuit must be analyzed to ensure that it is self-correcting.

(a) Use D flip-flops in the design.

(b) Use JK flip-flops in the design.

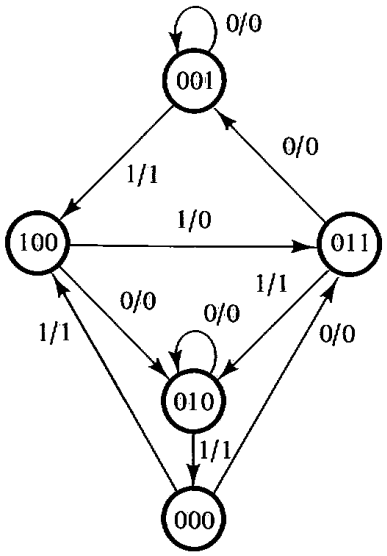


FIGURE P6-22

6-25 Design the following nonbinary sequence counters as specified in each case. Treat the unused states as don't-care conditions. Analyze the final circuit to ensure that it is self-correcting. If your design produces a nonself-correcting counter, you must modify the circuit to make it self-correcting.

(a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. Use JK flip-flops.

(b) Design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6. Use D flip-flops.

(c) Design a counter with the following repeated binary sequence: 0, 1, 3, 5, 7. Use T flip-flops.

(d) Design a counter with the following repeated binary sequence: 0, 1, 3, 7, 6, 4. Use T flip-flops.