Problem Set 7

1. A sequential circuit has two inputs x_1 and x_2 and one output z. Whenever an $x_1=1$ is observed, the output becomes *1* provided $x_2=1$ has been observed exactly twice since the last time $x_1=1$ was observed. The output remains *1* until $x_2=1$ is observed. Draw the state diagram as (a) a Mealy machine, and (b) as a Moore machine.

7-4 Design a sequential circuit whose state diagram is given in Fig. 6-31 using a 3-bit register and a 16 × 4 ROM.

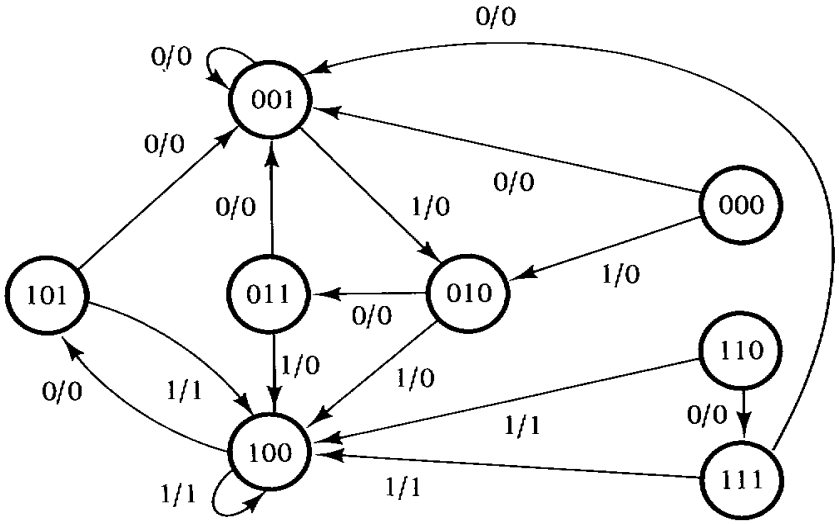

FIGURE 6-31
State diagram for the circuit of Fig. 6-30

7-9 Draw the logic diagram of a 4-bit register with four *D* flip-flops and four 4 × 1 multiplexers with mode-selection inputs s_1 and s_0. The register operates according to the following function table:

s_1	s_0	Register Operation
0	0	No change
0	1	Complement the four outputs
1	0	Clear register to 0 (synchronous with the clock)
1	1	Load parallel data

7-17 How many flip-flops will be complemented in a 10-bit binary ripple counter to reach the next count after the following count:
(a) 1001100111;
(b) 0011111111.

7-23 Design a synchronous BCD counter with *JK* flip-flops.

7-27 Using two circuits of the type shown in Fig. 7-19, construct a binary counter that counts from 0 through binary 64.

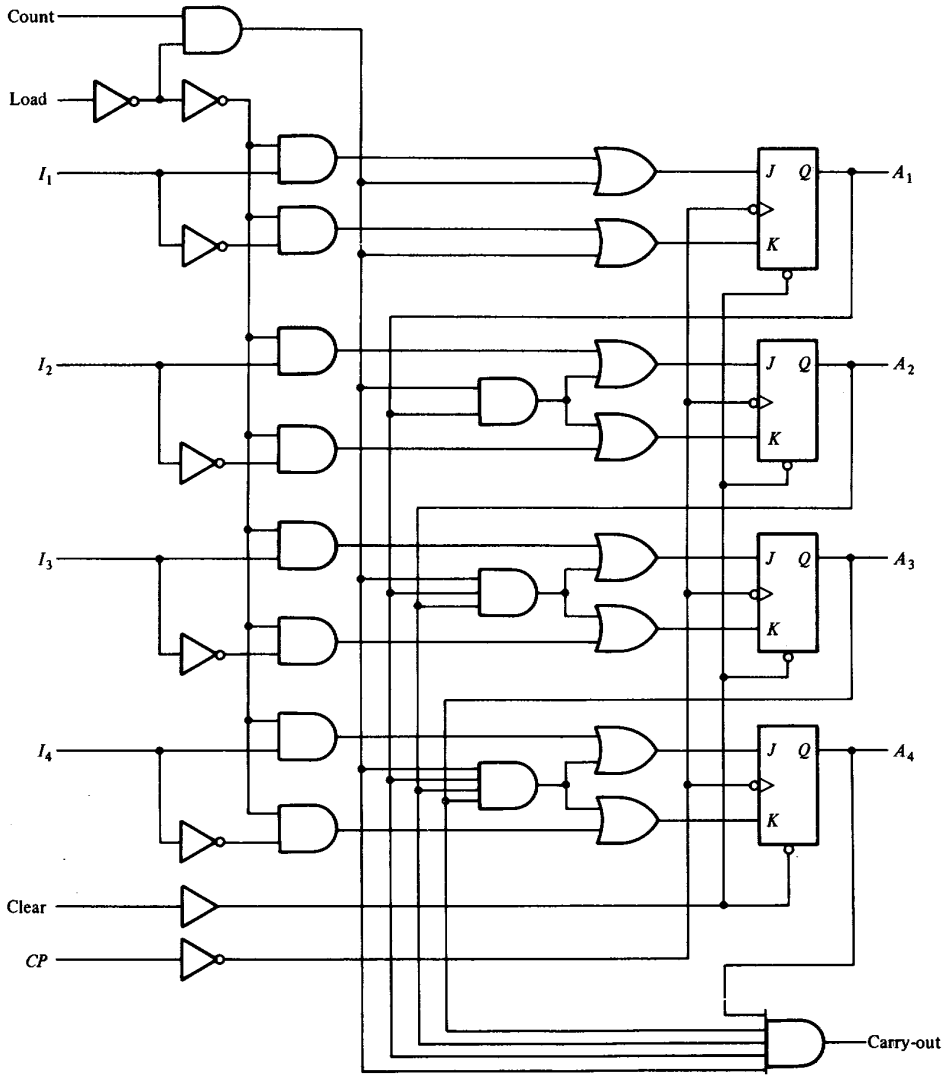

FIGURE 7-19
4-bit binary counter with parallel load