University of Waterloo Department of Electrical and Computer Engineering ECE 223 Digital Circuits and Systems Final Examination Winter 2000

Date April 12, 2000

Instructor: M. Sachdev

 Name
 Student ID
 Total

 1
 2
 3
 4
 5
 6
 7
 8
 9
 Total

Notes

1. Attempt all problems.

Duration 3 hours

2. If information appears to be missing make a reasonable assumption, state it and proceed.

3. Calculators are not needed and are not allowed.

4. No additional material is allowed.

Problem 1

(A): Convert following number from one radix to another [4] (127.094)₁₀ to radix 5

(B): Write a 4-bit gray code. In what applications usage of gray code is desirable? [4]

Problem 2

(A): What is the difference between Mealy and Moore machines [4]

(B): Highlight two major differences between a Programmable Logic Array (PLA) and a Programmable Array Logic (PAL) devices [4]

Problem 3

Simplify the following Boolean function by means of Quine-McCluskey tabulation method [12] P(A,B,C,D,E,F) = $\Sigma(6, 9, 13, 18, 19, 25, 27, 29, 41, 45, 57, 61)$

Problem 4

Design a combinational circuit that converts a binary number of 4 bits (WXYZ) to a binary coded decimal (BCD) format. Show the logic level implementation. **[12]**

Problem 5

Give a logic diagram of a level sensitive, master-slave flip-flop. Why edge triggered flip-flops are generally preferred in digital designs? Give a logic level diagram for an edge triggered flip-flop. [12]

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Problem 6

A sequential circuit is shown in the figure. Derive the state table and state diagram of the circuit [12]



Problem 7

Design a 4-bit ripple counter with Toggle flip-flops. What is the disadvantage of a ripple counter? [12]

Problem 8

Construct an ASM chart for a digital system that counts the number of people in a room. People enter the room from one door with a photocell that changes a signal x from 1 to 0 when the light is interrupted. They leave the room from a second door with a similar photocell with a signal y. Both x and y are synchronized with the clock but may stay on or off for more than one clock pulse period. The data processor subsystem consists of an up-down counter with a display of its contents. [12]

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Problem 9

Derive the transition table for the asynchronous sequential circuit shown in the figure. Determine the sequence on internal states Y_1Y_2 for the following sequence of inputs, $x_1x_2: 00, 10, 11, 01, 11, 10, 00$ [12]

