University of Waterloo
Department of Electrical and Computer Engineering
ECE 223 Digital Circuits and Systems
Final Examination
Winter 2001

Duration 3 hours | Instructor: M. Sachdev | Date April 9, 2001

Full marks 100

Name .... Student ID ....

1	2	3	4	5	6	7	8	9	Total

Notes

1. Attempt all problems.
2. If information appears to be missing make a reasonable assumption, state it and proceed.
3. Calculators are not needed and are not allowed.
4. No additional material is allowed.
5. Show all steps

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Problem 1

Convert following numbers from one radix to another [**8**]

(A): $(175.175)_{10}$ to binary

(B): $(7562.45)_{10}$ to octal

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Problem 2

A logic circuit implements the following Boolean function:

$$F = A'C + AC'D'$$

It is found that the circuit input combination $A = C = 1$ can never occur. Find a simpler expression for F using the proper don't care conditions. [**8**]

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Problem 3

Simplify the following Boolean function and implement it with a two level NOR gate circuit. Assume true as well as complement values of input variables are available. [**12**]

$$F(w,x,y,z) = \Sigma_m(5, 6, 9, 10)$$

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Problem 4

Design a combinational circuit that adds one to a 4 bit binary number, $A_3A_2A_1A_0$. For example, if the input of the circuit is $A_3A_2A_1A_0$ = *1101*, the output is *1110*. The circuit should be designed using four half-adders **[12]**

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Problem 5

Implement the following Boolean function with **a 4x1 multiplexer and external gates**. Connect inputs *A* and *B* to the select lines. The input requirements for the four data lines will be a function of variables *C* and *D*. These values are obtained by expressing *F* as a function of *C* and *D* for each of the four cases when *AB = 00, 01, 10, and 11*. [**12**]

$$F(A,B,C,D) = \Sigma_m(\mathbf{0, 1, 5, 8, 9, 11, 13})$$

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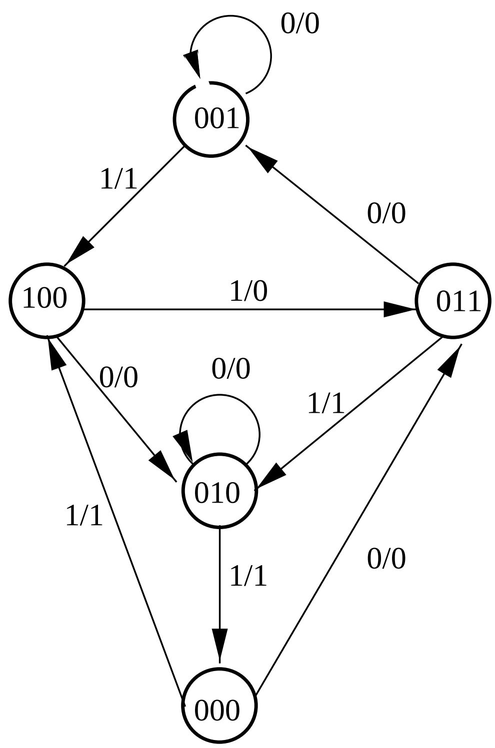
Problem 6

A synchronous, sequential circuit has three flip-flops, *A*, *B*, *C*; and one input *x*; and one output, *y*. The state diagram is shown in the figure. Design the circuit treating the unused states as don't-care conditions. Show the state table and draw the schematic **[12]**



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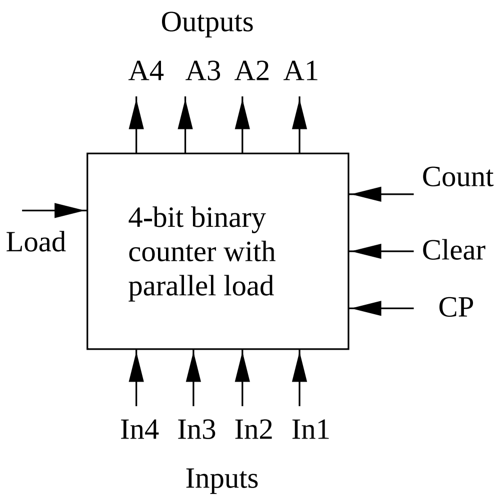
Problem 7

Using two 4-bit binary up counters (one is shown in the figure), construct a binary counter that counts from binary 4 through binary 99. [**12**]



Clear	Clock, CP	Load	Count	Function
0	X	X	X	Clear to 0
1	X	0	0	No change
1	↑	1	X	Load input
1	↑	0	1	Count next binary state

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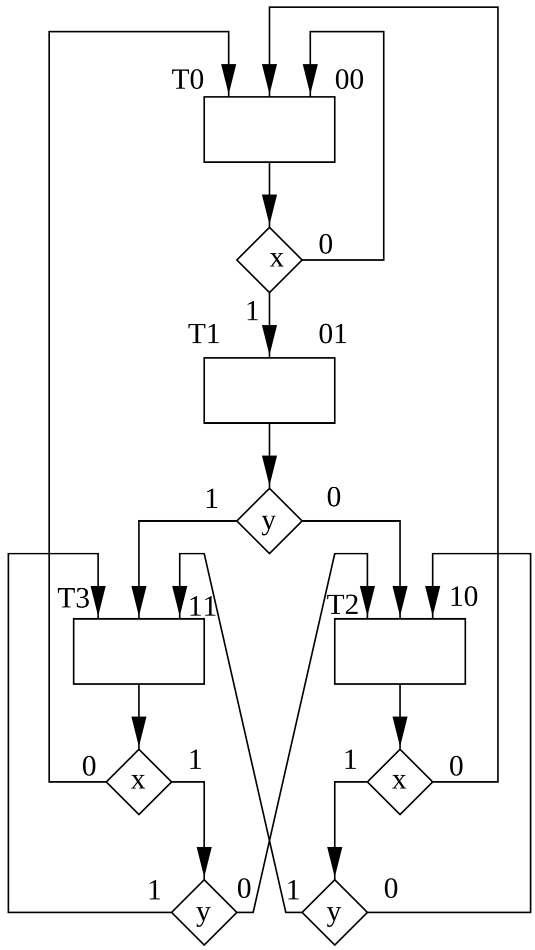
Problem 8

An ASM chart is illustrated in the figure. Construct the state table for the controller. Draw the synchronous, sequential circuit with D flip-flops and combinational logic. [**12**]



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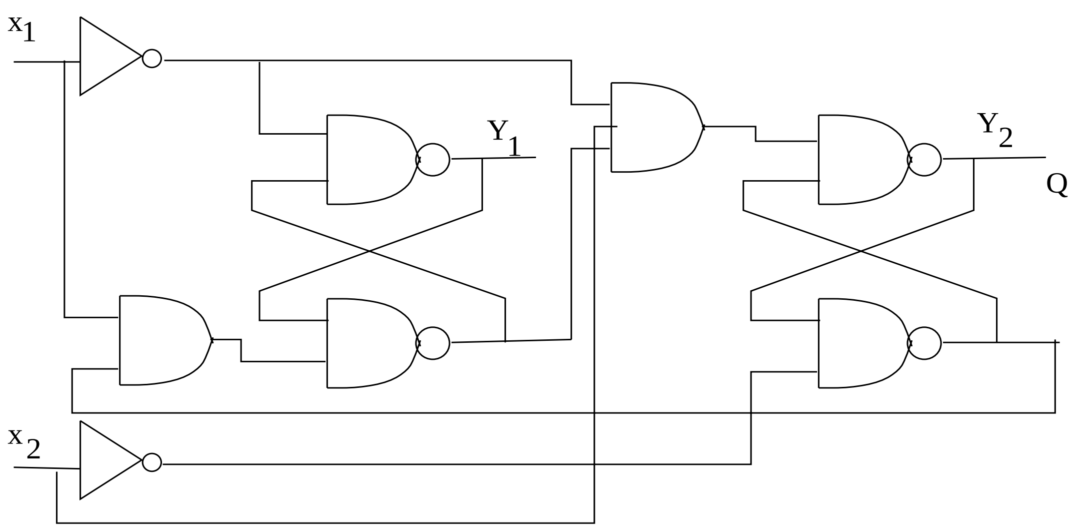
Problem 9

An asynchronous sequential circuit is shown in the figure:

(i) Derive the Boolean functions for the outputs of the two SR latches Y_1 and Y_2.

(ii) Derive the transition table and derive the output map for output Q of the circuit. [**12**]



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