E&CE 437
Integrated VLSI Systems

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Lecture Transparencies

(Introduction)

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Course Details

- **Instructor:** M. Sachdev, msachdec@ece.uwaterloo.ca
- **TA:** Bhaskar Chatterjee, bhaskar@vlsi.uwaterloo.ca
- **Lectures:** tuesdays & thursdays (2.30 - 3.20 in MC2034)
- **Tutorial:** thursday 4.30 - 5.20 in MC 2038
- **Text:** Digital Integrated Circuits, Jan Rabaey, Printice-Hall, 1996
- **Grading:** Project 30%; mid term 20%, final 50%

Course Outline (1 of 3)

- **Introduction (1)**
  - Basic properties and trends in digital ICs
- **MOS transistor (3)**
  - NMOS,PMOS transistors, operational modes, I-V characteristics, DC & transient behavior, models, short channel effects
- **Inverter (3)**
  - Properties, static and dynamic behavior, power, energy consumption, and Power-Delay product (PDP)
- **CMOS combinational logic design (3)**
  - Static CMOS, pass transistor logic, dynamic logic, noise considerations, power consumption in CMOS gates

Course Outline (2 of 3)

- **CMOS sequential logic design (3)**
  - Static sequential logic, dynamic sequential logic, TSPC
- **CMOS arithmetic circuits (5)**
  - Datapaths, adder circuit and architecture design, multiplier architecture and circuit design
- **Clocking strategies (3)**
  - Single phase, two phase, clock generation and propagation, clock skew
- **VLSI Interconnects (4)**
  - modeling of interconnect capacitance and resistance, IR drop, electromigration

Project (1 of 2)

- **Computer accounts for project**
  - Accounts will ne setup in VLSI labs to run CADENCE; You will have to sign NDA to CMC; Your accounts will be issued to you once you hand your project proposal in 3rd tutorial
- **Project topics**
  - Design and layout of a reduced swing clock network
  - Design and layout of a low power, 16 bit adder
  - Design and layout of a high performance, 16 bit adder
  - Design and layout of a 6x6, pipelined multiplier
- **Project requirements**
  - Team of 3 individuals per project (30 hours/individual)

Project (2 of 2)

- All projects should involve, circuit schematic, transistor sizing, simulation, layout, DRC, LVS
- **Deadlines**
  - **1 page proposal that states:** objectives, project outline, milestones, workload distribution (week 3, tutorial)
  - 1 page progress report: (week 7, tutorial)
  - project report: (week 12, tutorial)
  - Single report should be submitted per project, report **not** to exceed 25 pages)

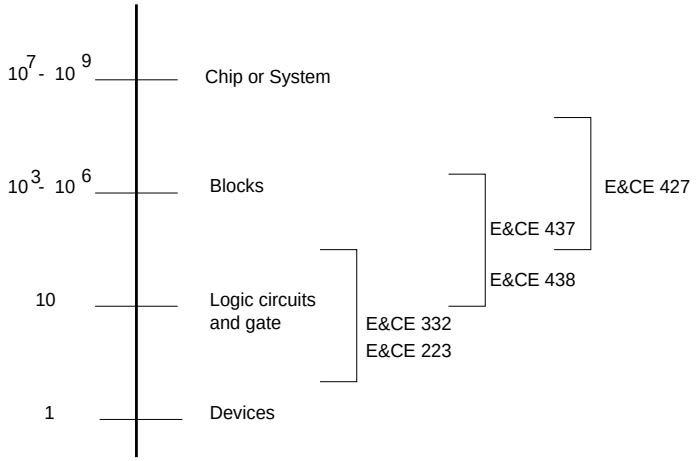
Introduction

- **Digital signals**
  - Have discrete values (typically 0,1)
  - Unlike analog signals which have continuous values
- **Digital circuits**
  - Obey Boolean algebra
  - consists of combinational (INV, NAND, NOR) and sequential (flip-flops, latches) logic gates
- **Digital systems**
  - Manipulate discrete data and produce discrete results
  - Unlike analog systems, digital systems are easier to analyze and design

Technology Projections, SIA 1997

year of first DRAM shipment	1997 (0.25)	1999 (0.18)	2001 (0.15)	2003 (0.13)	2006 (0.10)	2009 (0.07)
DRAM	64M	256M	1G	4G	16G	64G
No of pads (high perfor)	1450	2000	2400	3000	4000	5400
No. of packaged pin						
microprocessor	600	810	900	1100	1500	2000
ASIC (high perfor)	1100	1500	1800	2200	3000	4100
Chip frequency (MHz)						
On chip, local clock (hi. perf)	750	1250	1500	2100	3500	6000
On chip, glo. clock (hi. perf)	750	1250	1400	1600	2000	2500
On board (hi. perf)	250	480	785	885	1035	1285
Chip Size (mm^2)						
DRAM	280	400	445	560	790	1120
Microprocessor	300	340	385	430	520	620
ASIC	480	800	850	900	1000	1100
Wiring levels	6	6-7	7	7	7-8	8-9

This Course



Rationale and Objectives

- **In spite of significant advances in design automation tools and modular design practices, we have still to be concerned about intricacies in design**
  - Device and circuit level issues become significant if low power or high performance is desired
- **Objective is**
  - To develop insight of technology evolution and scaling
  - To familiarize with custom or application specific design style