Design and Modeling of High-Impedance Electromagnetic Surfaces for Switching Noise Suppression in Power Planes

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***Abstract*—This paper presents a detailed design and modeling approach for power planes with integrated high-impedance electromagnetic surfaces (HIS). These novel power planes, which were introduced recently, have the unique ability of providing effective broadband simultaneous switching noise (SSN) mitigation. Full-wave electromagnetic simulation is used to study the impact of the geometry on the performance of these novel power planes. It is demonstrated that power planes using inductance-enhanced HIS can be designed for broadband mitigation of the SSN from the upper hundred megahertz to the gigahertz frequencies. Physics-based compact models for the unit cell of power planes with integrated HIS are developed and several of them connected in a two-dimensional array to build full models for large and multilayer power planes. The compact model offers fast analysis of power planes. As an example, we show that the full-wave simulation time of a 10 $\times$ 10 cm power plane with integrated HIS can be dramatically reduced from 24 to 48 h using a commercially available three-dimensional full-wave solver to less than 1 min when using the compact circuit model developed here.**

***Index Terms*—Electromagnetic band-gap structures, high-impedance surface, simultaneous switching noise, switching noise.**

I. Introduction

With the continuous downscaling of MOSFETs, the increasing gate density and the increasing clock frequency in modern microprocessors, simultaneous switching noise (SSN) has become a major concern. When many active devices switch at the same time, the noise generated can cause fluctuations or disturbances in the power distribution system, which in turn leads to a degradation of the signal integrity [1]–[3]. This problem of SSN, also known as delta-I noise or power/ground bounce, has been discussed intensively over the past decade and different approaches have been taken to mitigate it. (For a representative sample of the literature, the reader is referred to [2]–[4] and references therein.) In printed-circuit-board (PCB) technology, the most common approach of mitigating SSN consists of using discrete decoupling capacitors around sensitive integrated circuits [4]–[9], whereby most of the recent work has focused on optimizing the number and the location of these capacitors on the PCB. These capacitors are usually connected between the power and the ground planes and are expected to behave as a short circuit between the two planes at high frequencies. It has been found, however, that the lead inductance of these real capacitors strongly limits their noise mitigation capability. In fact, with their parasitic lead inductance, real capacitors used today in PCBs act as series resistance-inductance-capacitance (*RLC*) resonant circuits. In fact, the capacitor becomes a short circuit only around its self-resonant frequency and an open circuit at all other frequencies. An alternative to discrete capacitors is embedded capacitance, which is obtained by significantly reducing the separation between the $V_{\rm dd}$ and the ground planes [10]–[12]. Embedded capacitance shows slightly better high frequency performance because of the absence of lead inductance; however, most of the limitation to this technology is given by the costs and the fragility associated with the thinning of the PCB.

Other less used techniques, which have been demonstrated for SSN mitigation in power planes, include the use of differential interconnects, which inherently reject the common mode noise [13], and the etching of trenches around sensitive active devices as described in [14]. In the latter, the isolated active device area is connected to the rest of the power plane via small inductors. The techniques discussed above are selectively implemented during the fabrication of the PCB or in a postprocessing step. This contributes to an overall cost increase of the PCB. In addition they offer only localized solutions for noise mitigation.

Most recently, a novel concept of mitigating SSN using a high-impedance electromagnetic surface (HIS) or an electromagnetic band-gap structure (EBG) in place of the ground plane was introduced [15], [16]. Contrarily to the previously known techniques, this new concept is expected to offer an efficient blockage of the SSN all over the HIS and in all directions. This blockage or trapping of propagating waves occurs when the HIS is designed such that its forbidden band-gap contains the frequency range where the simple power plane is in its dominant mode of resonance. In a previous work [15], we briefly introduced the concept of inductance-enhanced high-impedance surfaces and combined it with *RC* decoupling capacitors for broadband noise mitigation.

The purpose of the present work is to investigate the qualitative relationships between the geometrical and the electrical attributes of both power planes with standard and inductance-enhanced HIS and to develop a lumped-element compact model that would facilitate the use of these power planes in circuit simulators. First, the origin of resonant modes

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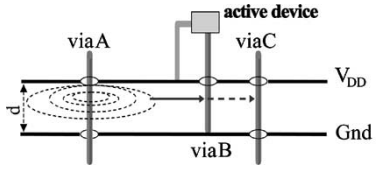

Fig. 1. Traditional power plane pair with connecting vias.

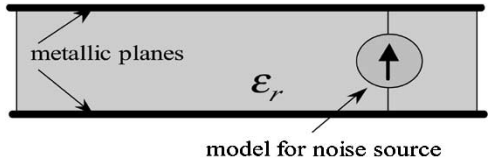

Fig. 2. Full wave model of a traditional power plane with noise source.

in the power plane system is discussed. Electromagnetic (EM) simulation capability is then established by achieving a good match with measured data in terms of S-parameters for a simple power plane. A number of simulations are then performed on power planes while varying the main physical (geometrical) parameters. A lumped-element compact model is then developed and used to study the noise transmission at various locations on the power plane. The combination of the HIS with decoupling capacitors for broadband noise mitigation is also studied.

II. Origin and Analysis of SSN in Traditional Power Planes

A. Resonant Modes in Power Planes

Today's computer systems and microprocessors utilize multilayer PCBs. Some of these layers are used for signals, whereas others are used for power distribution. In many PCBs the power is distributed on several layers. The minimum requirement for the power distribution network, however, is to have at least two planes as shown in Fig. 1, where one plane is connected to the supply voltage $V_{\rm DD}$ and the other plane is connected to the reference voltage $V_{\rm ref}$ or ground (Gnd). The two power planes extend over the entire width and length of the PCB and, therefore, constitute a parallel-plate waveguide. At different locations, integrated circuits (ICs) containing mostly active devices are connected between the two planes as illustrated by the active device on via B (Fig. 1). At some locations, the active devices are connected to the signal layers using through-vias as illustrated by via A. When the active device on via A, for example, switches, a sudden change of current consumption occurs at that location. One or more modes of the parallel-plate waveguide will be excited, causing voltage waves to propagate from via A through the waveguide system. These voltage waves would then affect the $\rm V_{DD}$ on the board, which in turn can lead to the disturbance of the voltage of the active device connected to via A itself or to that of other active devices on the board. In this case, the problem of mitigating SSN in power planes is reduced to suppressing resonant modes in a parallel-plate waveguide with finite width and length.

The parallel plate waveguide consisting of two planes can support transverse electromagnetic (TEM), transverse magnetic (TM), and transverse electric (TE) waves [17]. With the thickness of the planes considered in this work being on the order of 1–5 mm, the TM and TE waves have cutoff frequencies on the order of hundred gigahertz, as the cutoff frequencies for both $\rm TM_{\it m}$ and $\rm TE_{\it m}$ waves are given by (1), where m is the mode number and d is the separation between the two plates. The dominant wave modes are the TEM modes with the cutoff frequency corresponding to that of $\rm TM_0$ [14]. The frequencies

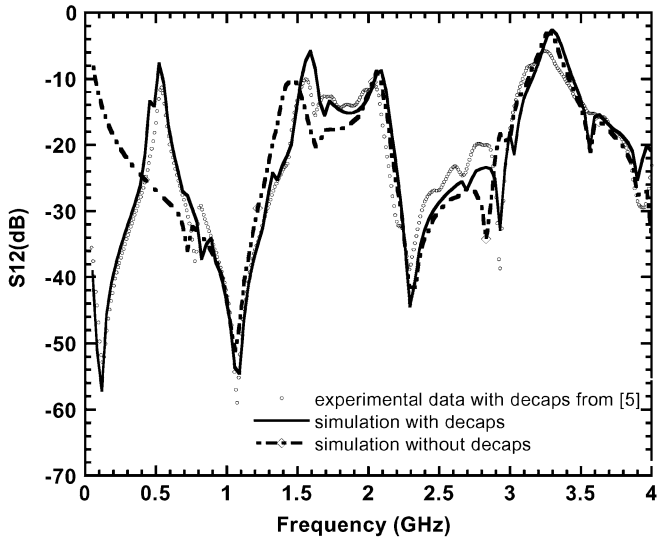

Fig. 3. Measured versus simulated magnitude of S12 of a 10×10 cm power plane with and without decoupling capacitors. The ports are located at (5 cm, 2 cm) and (5 cm, 5 cm).

of the excited TEM modes can be approximated by (2). Here a and b represent the width and length of the parallel plates, whereas m and n represent the mode numbers

$$f_m = \frac{m}{2d\sqrt{\mu\varepsilon}} \tag{1}$$

$$f_{mn} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}. \tag{2}$$

From (2) it is clear that the number of resonant modes for a given frequency range increases with the size of the parallel plates. In other words, the resonant modes shift to lower frequencies with increasing plate dimensions.

Fig. 2 shows the simplified model used for the traditional power plane analysis. The two planes are represented by two solid metallic plates, separated by dielectric material. The connecting via which is actually the source of the radiating waves (or noise source) is replaced with an ideal current source. The performance of the power plane is evaluated by calculating the S-parameters, which gives the power transfer from the noise source to any load located on the power plane. The simulation is performed in a 50-Ω environment.

Ansoft HFSS [18], a finite element method (FEM) based EM simulator, is used for the analysis. The validation of the simulator is established by comparing the S-parameters generated through measurement and simulation for a reference structure. Fig. 3 shows the comparison with respect to S-parameters of a 10×10 cm power plane with and without decoupling capacitors for noise mitigation as described in [5]. The total height

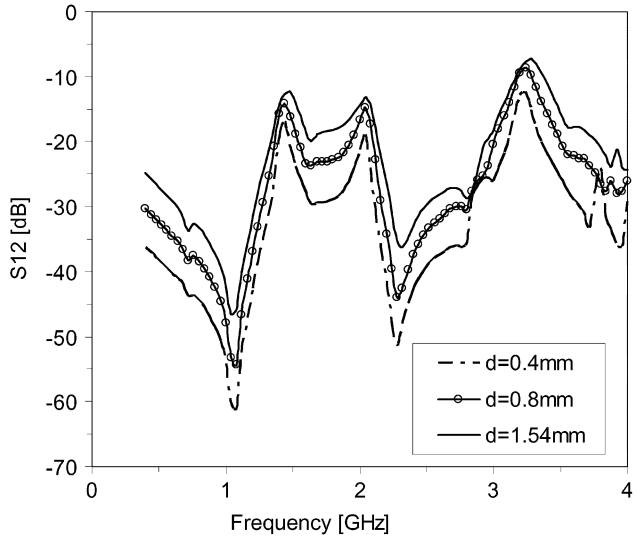

Fig. 4. Effect of plate spacing on traditional power plane switching noise. The port locations are the same as in Fig. 3.

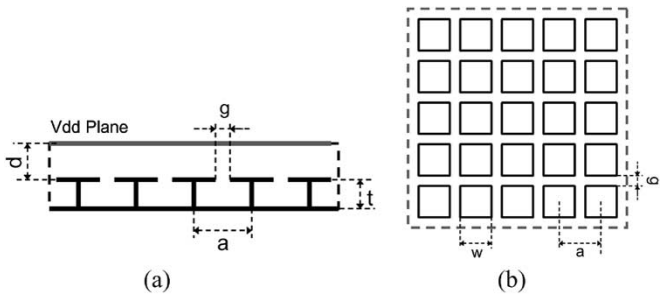

Fig. 5. Geometry of the power plane with embedded HIS structure: (a) cross section and (b) top view.

of the power plane is 1.54 mm, and the dielectric constant is 4.4. The parasitic inductance and resistance of the decoupling capacitors are also taken into consideration. The power plane without decoupling capacitors exhibits very high transmission at low, intermediate, and high frequencies. A very good match can be seen over the entire frequency range between the measured and the simulated data. As expected, the decoupling capacitors are only effective at low frequencies ($<$500 MHz), where the impedance associated with the lead inductance of the discrete decoupling capacitors is negligible. Even as the board height is decreased to the submillimeter dimensions, only very low frequency SSN associated with the board parasitic inductance is mitigated while the fragility and associated reliability are worsened. As illustrated in Fig. 4, high-frequency noise associated with the finiteness of the lateral dimensions of the board as stated in (2) remain almost unchanged.

III. Power Planes Using HIS With Straight Vias

A. Power Plane Geometry

Fig. 5 shows a typical power plane with integrated HIS, where the bottom plate or ground plane of the traditional power plane (Fig. 1) has been replaced with a HIS. The HIS has the ability

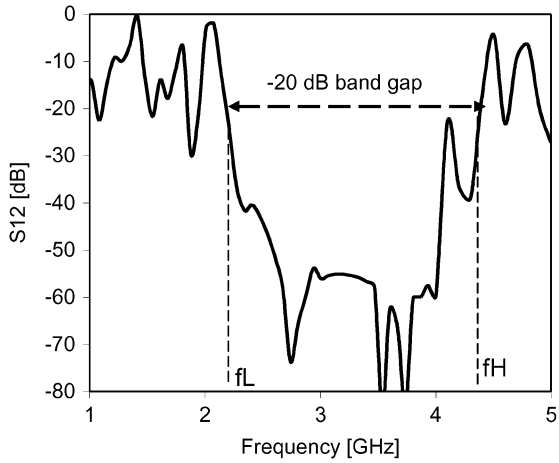

Fig. 6. Typical insertion loss of finite size parallel-plate waveguide loaded with periodic HIS showing the -20-dB band gap and the corner frequencies.

of stopping surface wave propagation on a given frequency band [19]. It consists of polygonal metallic patches connected to a bottom metallic plate through straight metallic posts (vias) with a square or circular cross section and filled with dielectric material. The key geometrical parameters of the power plane system include the via to via distance or periodicity a of the HIS, the via height t, the separation or gap g between the patches, the patch width w, and the thickness d of the dielectric material between the HIS and the top or $V_{\rm DD}$ plane.

B. Power Plane Characterization

Once the simulation capability is established, physical parameters of interest are varied to find the optimized noise mitigation capability or to analyze the parameter sensitivity. To illustrate this, the geometrical parameters t and g are varied and the resultant changes of the S-parameters are evaluated.

Fig. 6 illustrates the insertion loss S12 of a typical power plane with integrated HIS. In this and in other analysis in this section, the noise source is located at (4.5 cm, 4.5 cm) and the receiving port is at (4.5 cm, 1.5 cm). These port locations were chosen in the reference structure to allow a one-to-one comparison with the experimental results of the traditional power plane reported in [5]. From the S12 curve, which is indeed the frequency response, an x-dB (-20 dB in this case) bandwidth, with lower and upper corner frequencies f_L and f_H can be defined, where x represents the level of the insertion loss. The other characteristics of the power plane, which are the center frequency, f_0, the fractional bandwidth, ΔBW, and the absolute bandwidth, BW, can then be obtained as follows:

$$f_0 = \frac{f_H + f_L}{2} \tag{3}$$

$$\mathrm{BW} = f_H - f_L \tag{4}$$

$$\Delta\mathrm{BW} = \frac{\mathrm{BW}}{f_0} = \frac{2(f_H - f_L)}{f_H + f_L}. \tag{5}$$

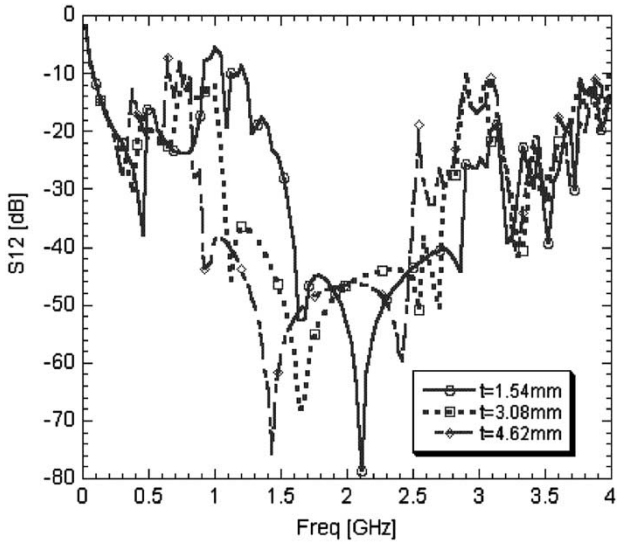

Fig. 7. Effect of via length on frequency response.

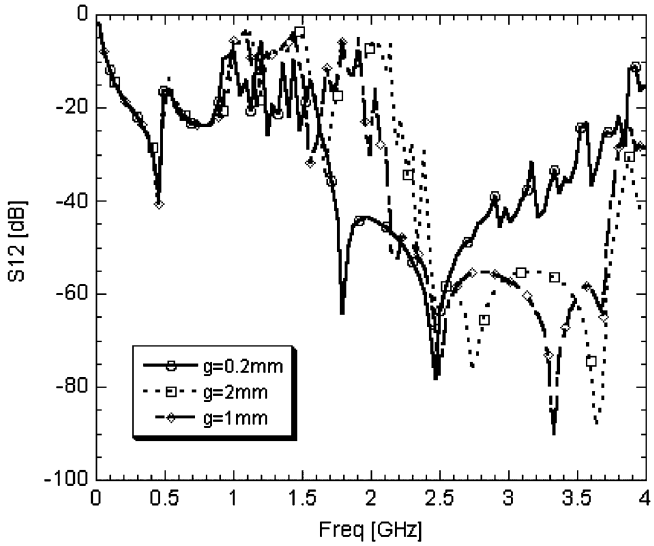

Fig. 8. Effect of patch separation on frequency response.

C. Effect of Via Height

The first parameter to be studied is the via height. Fig. 7 shows the frequency response when the via height is varied from 1.54 to 4.62 mm. All other geometrical parameters are fixed. In this case $g = 150$ μm and $a = 10$ mm. When t increases, the center frequency as well as the corner frequencies of the stopband are shifted to lower frequencies. This decrease of the center frequency is associated with the increase in inductance, which is proportional to the via length. The self-resonance frequency of the HIS is given as

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{LC}} \tag{6}$$

where L and C represent the sheet inductance and sheet capacitance of the HIS, respectively [19]. At the same time the fractional bandwidth increases. This is attributed to the fact that it is proportional to

$$\Delta\text{BW} \sim \sqrt{L/C}. \tag{7}$$

It is also important to notice that a significant increase of the via height is necessary to achieve noise mitigation in the hundreds MHz range.

D. Effect of Patch Separation

The patch separation g is varied from 2 to 0.20 mm with the via height fixed at 1.54 mm. All other geometrical parameters are kept constant. The distance between the HIS and the top plate is fixed at 1.54 mm. A decrease Δg of the spacing corresponds to an increase $\Delta w = \Delta g$ of the patch width. When the spacing g decreases, the fringing capacitance between adjacent patches increases, which in turn leads to an overall increase of the HIS sheet capacitance. This implies a decrease of both the center frequency and the fractional bandwidth according to (6) and (7). Fig. 8 shows the impact of varying the patch spacing on the power plane performance.

E. Systematic Analysis of the Power Plane Geometrical Parameters

1) Analysis Using Dispersion Diagrams: Dispersion diagrams show the relationship between wave numbers and frequency. These diagrams present propagating modes and band gaps that can potentially exist between such modes (in a periodic structure at a given frequency of operation, many modes in different directions may be excited) [20]. Brillouin, in his theory of wave propagation in periodic structures [21], states that for any periodic structure there are certain vectors (i.e., directions) in the unit cell of the periodic structure that constitute a boundary region called irreducible Brillouin zone. According to this theory, deriving the propagating modes in the direction of these vectors suffices to cover all the possible directions of propagation within the lattice. Hence the problem of deriving the propagating modes excited at a certain frequency reduces to finding such modes only in the directions of the vectors of the irreducible Brillouin zone. For the type of structure considered in this work, the border of the irreducible zone is illustrated in Fig. 9 and it consists of the vectors pointing from Γ to X, from X to M, and from M back to Γ.

Therefore, in light of Brillouin theory, a dispersion diagram will consist of three regions. The first one is the one in which only propagation in the x direction is considered. In this direction, the wave number will correspond to k_x, which in turn translates into the phase shift between the two sides of the unit cell shown in Fig. 9 for a wave propagating in the x direction. This translation allows the derivation of dispersion diagram using traditional eigenmode full-wave simulators. In these simulations, the unit cell structure and required phase shifts are given to the simulator. The simulator calculates the frequencies of propagating waves that would generate such phase shifts. For a wave propagating in the x direction with no y variation, phase 1 varies between 0 and 180 $^\circ$ and phase 2 is kept constant at zero degrees. This corresponds to the Γ to X direction. The X to M vector corresponds to phase 1 constant and equal to 180 $^\circ$ and phase 2

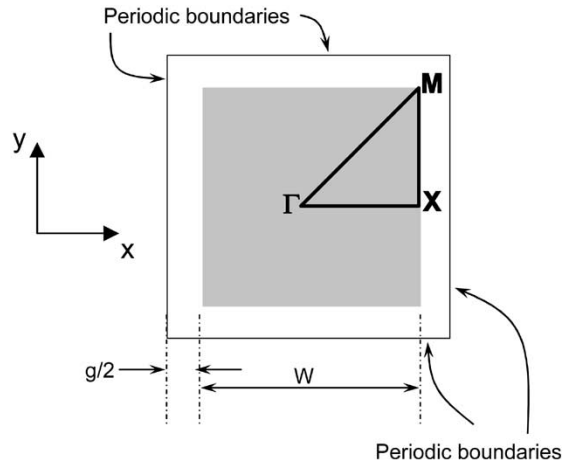

Fig. 9. Top view of the unit cell of a periodic HIS showing the Brillouin triangle.

TABLE I
SUMMARY OF DESIGNS USED FOR ANALYZING THE FUNDAMENTAL LIMITATIONS OF POWER PLANES WITH INTEGRATED HIGH-IMPEDANCE ELECTROMAGNETIC SURFACES. THE SAME DESIGNS ARE ALSO REPEATED FOR $g = 0.8, 1.2$, AND 2 mm

Design Number	a[mm]	T mm]	d [mm]	g [mm]
1	3	1.54	1.54	0.4
2	5	1.54	1.54	0.4
3	8	1.54	1.54	0.4
4	10	1.54	1.54	0.4
5	15	1.54	1.54	0.4
6	20	1.54	1.54	0.4

varying from 0 and 180 °. This represents the second region in the dispersion diagram. The third region is represented by the M to Γ direction in which both phases are equal and changing from 180 ° back to zero. For the case of wave propagation in free space, as there is no dispersion, the diagram will consist of a straight line in the first and third regions. In the second region the relationship is quadratic.

In the previous sections it was verified that the operating frequency of power planes with integrated HIS could be decreased either by increasing the via height or by reducing the spacing between adjacent patches. To further understand what the fundamental limitations of power planes with integrated HIS are, the period a and the spacing g are varied systematically and the Γ-X section of the dispersion diagram extracted for each structure. A variation of the period with fixed gap between the patches corresponds to a simultaneous variation of the patch width. The electrical characteristics of interests, which are the center frequency, the lower corner frequency, the upper corner frequency, and the absolute and the fractional bandwidths are then derived from the dispersion diagram. The study assumes an FR4 substrate with dielectric constant of 4.4 and a standard PCB technology, where the thickness of each substrate laminate is 1.54 mm. Table I shows the list of designs used in the simulation.

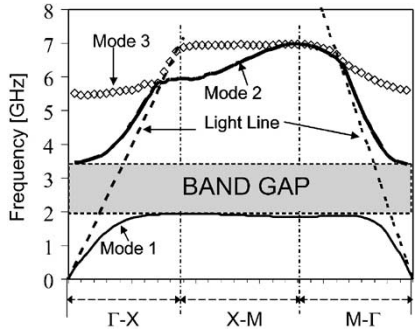

Fig. 10. Full dispersion diagram of infinite power plane with integrated HIS. $a = 10$ mm, $g = 1$ mm, $h = d = 1.54$ mm, $\varepsilon = 4.4$.

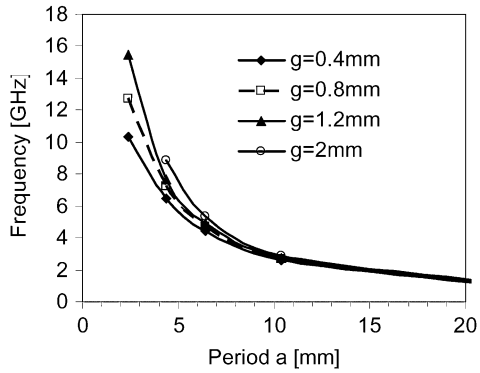

Fig. 11. Dependence of the band gap's center frequency on period and gap spacing.

The extraction of the dispersion diagram of the power plane is much faster than the full-wave simulation of the S-parameters since it is based on the analysis of a single cell. It, however, has the limitations that it does not provide the level of signal attenuation and it only gives the characteristics of infinitely large periodic structures. Using a unit cell similar to that of Fig. 9, eigenmode solutions for Maxwell equations are determined under assumption of perfect electric boundary conditions at the conducting boundaries ($V_{\rm dd}$ and ground plates in the z-direction) and periodic boundary conditions in the xy-plane. The phase constant is varied along the reduced Brillouin triangle Γ-X-M, while solving for the first N eigenmodes. A detailed extraction procedure is reported in [22].

The resulting dispersion diagram for the sample unit cell of Fig. 9 is shown in Fig. 10. A frequency band gap, where the infinite structure does not allow any wave propagation, can be seen between the first and second modes. This information is sufficient to derive the power plane characteristics described by (3)–(6). In addition to the first three eigenmodes, the dispersion diagram also includes the light line, whose slope corresponds to light velocity along a different axis in that medium.

2) Simulation Results: Fig. 11 shows the center frequency versus period, where the gap g is used as a parameter. An increase in the period (with constant g) corresponds to an increase in the patch dimensions, which effectively increases the sheet capacitance of the HIS. This leads to a decrease of the center frequency. Figs. 12 and 13 show the upper and lower corner

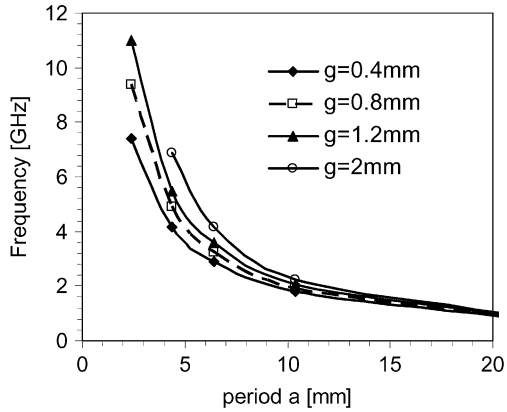

Fig. 12. Dependence of the band gap's lower corner frequency on the period and gap spacing.

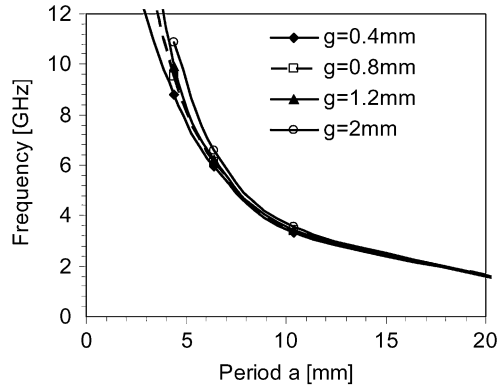

Fig. 13. Dependence of the band gap's upper corner frequency on the period and gap between the patches.

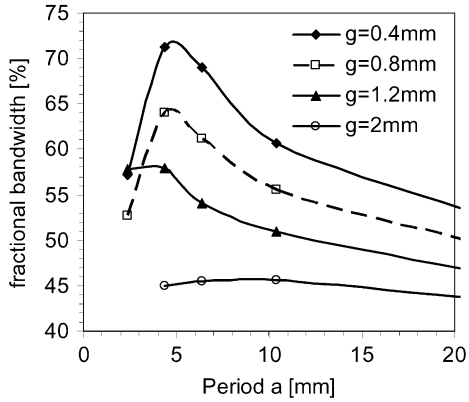

Fig. 14. Dependence of the fractional bandwidth on the period and gap between the patches. Numerical error can explain the discrepancy seen for $g = 1.2$ mm.

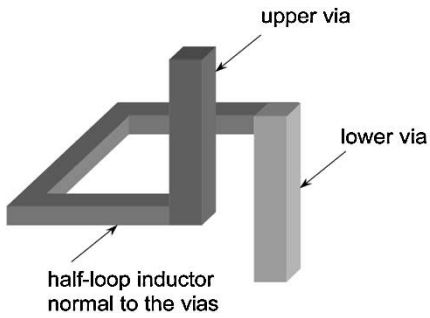

Fig. 15. Single-loop inductor for inductance enhancement.

frequencies of the stopband versus period, where the gap is used as a parameter. The period has the most impact on the location of the upper corner frequency, as was discussed in [23] for capacitance-enhanced photonic band-gap structures (PBGs). The lower corner frequency on the other hand changes mostly with the gap, indicating its strong dependence on the lumped behavior of the high-impedance surface. For the substrate thickness considered, a period of about 15 mm is needed to realize band gaps with center frequency below 2 GHz. In this case the absolute bandwidth is on the order of only a few hundreds megahertz.

Fig. 14 shows the fractional bandwidth versus period. It starts at a low value, increases to a maximum, and then decreases again. As the period increases, both the inductance of the patch and the fringing capacitance between adjacent patches increase. When the width of the patch is much larger than the via height, the total inductance of the patch saturates against the sheet inductance of a regular parallel-plate wave guide given by [17]. This results in a saturation of the total sheet inductance, which is equal to the sum of the patch and via inductances. At this point the fractional bandwidth is at its maximum. Any increase of the period beyond this value only increases the sheet capacitance, which then leads to a decrease of the fractional bandwidth.

IV. Power Plane Using Inductance-Enhanced High-Impedance Surface

A. Power Plane With Single-Loop Inductor in the HIS

As discussed in the previous paragraph, the use of a HIS with straight vias in power planes has two main limitations for low gigahertz noise mitigation. First, large via lengths are required for lower frequencies. This increases the thickness, weight, and cost of the power planes. Second, the achievable fringing capacitance between the patches is limited by the minimum metal-to-metal spacing that most PCB technologies can offer. Capacitance-enhanced HIS were proposed in [19] and used in [16] for parallel-plate mode suppression in high-speed systems. Although the capacitance enhancement shifts the noise stopband to lower frequency, it also leads to a decrease of the fractional bandwidth. In [15], we proposed and used inductance-enhanced HIS for SSN mitigation in high-speed digital circuits. In that work, and as illustrated in Fig. 15, the single straight via of the HIS is replaced by a novel inductive element, which can be used to control the sheet inductance of the HIS.

With the total thickness of the power plane system (including the HIS) fixed at 1.54 mm, the length l of the single-loop inductor was varied from 5 to 16 mm. Fig. 16 shows the insertion loss for the two extreme cases. If we consider the -30dB bandwidth as the stopband of the power plane, we notice that the fractional bandwidth increases with the loop length. At the same time there is a decrease in the bandwidth, suggesting that for

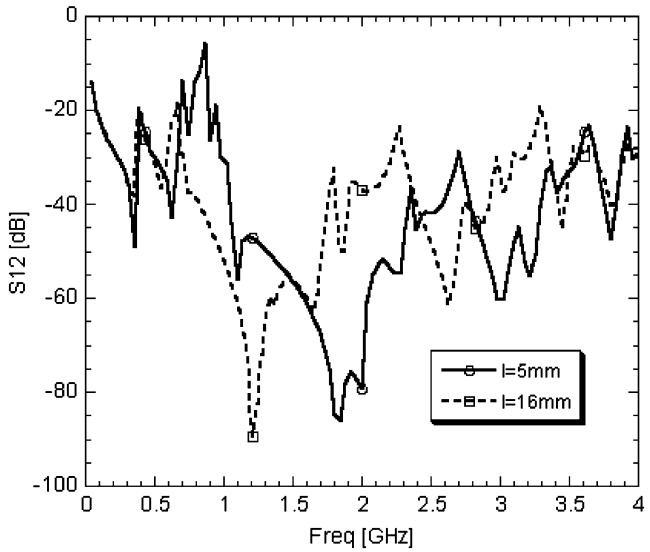

Fig. 16. Effect of inductor loop length on insertion loss.

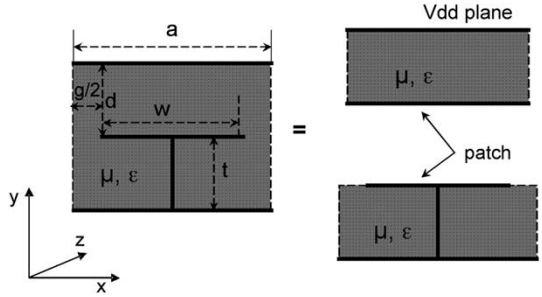

Fig. 17. Cross-sectional view and decomposition of power plane unit cell into a parallel-plate transmission line and HIS cells.

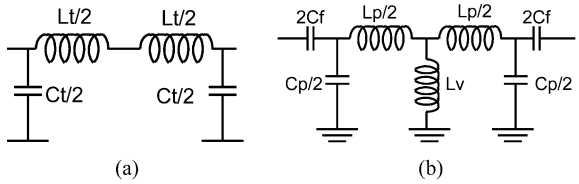

Fig. 18. Equivalent circuits of (a) parallel-plate transmission line and (b) HIS unit cell for one-dimensional wave propagation. Conductor and dielectric losses are not shown.

any given structure the noise mitigation capability would also saturate as the inductance increases. More important, resonance suppression is achieved down to 700 MHz without any increase of the power plane thickness.

B. Power Plane With Multiturn Inductor in the HIS

Instead of using a single-loop inductor, a multiturn inductor can be used to enhance the sheet inductance of the HIS. By using a multiturn or spiral inductor, the inductance per unit area is increased significantly. This is especially important if SSN mitigation below 1 GHz is desired. Because the area required by the inductor is very small, unwanted inductive coupling with adjacent cells is also minimized. The frequency behavior of the power plane is very similar to that of the power plane with single-inductor loop.

V. Compact Model Development

A. Model Form Definition

Lumped-element equivalent circuits have been demonstrated for traditional power planes [24]–[26], but none has been proposed for parallel-plate waveguides with integrated HIS. The only model that exists for stand-alone HIS is based on the transmission line theory and is developed for two main directions of wave propagation [27]. This model assumes the use of straight vias and rectangular patches. In this work, the compact model of the power plane is developed by first dividing it into unit cells. Each cell is modeled individually and multiple cells are then connected into a two-dimensional array to construct the compact model for the full power plane. For power planes with HIS, the boundaries of the unit cell are predefined by the periodicity of the HIS.

Fig. 17 shows the cross-sectional view of the power plane unit cell and its decomposition into two effective cells for the HIS and the section between the HIS and the $V_{\rm dd}$ plane. The latter can be approximated by a parallel-plate transmission line, whereby it is important to note that the reference for this transmission line is the patch of the HIS. For one-dimensional wave propagation the parallel-plate transmission line cell can be modeled with the equivalent circuit of Fig. 18(a), where Lt is the total inductance of the $V_{\rm dd}$ plane and Ct is the total capacitance between the patch and the $V_{\rm dd}$ plane. Similarly the HIS cell can be modeled for one-dimensional wave propagation using the equivalent circuit of Fig. 18(b), where Lp is the total inductance of the patch, Lv is the via inductance, Cp is the total capacitance between the patch and the bottom plate of the HIS, and Cf is the fringing capacitance to the adjacent unit cell. The total capacitance between the $V_{\rm dd}$ plane and the bottom of the HIS as well as the mutual inductance between adjacent cells, which are not shown directly, are redistributed in the other components of the model. Also conductor and dielectric losses are included in the model by adding resistance in series with the inductance and conductance in parallel to the capacitance, respectively.

For two-dimensional wave propagation, the same model forms of Fig. 18(a) and (b) are used for the other main direction of propagation since the cells are square and symmetric. This results in a four-port compact model for both the transmission line and the HIS cells. The cascading (stacking) of the two individual unit cell models results in the model of the power plane unit cell shown in Fig. 19. Here, a resistance has been added in series to each inductance piece to account for the skin effect losses. In general, a conductance can be added in parallel to each capacitance in the model to account for the dielectric losses. The compact model of a full power plane can then be obtained by connecting several of this unit cell models into a two-dimensional array. This compact model form is very generic and can be used for power planes with integrated inductance- or capacitance-enhanced HIS as well. In general, when the polygonal patch has n sides, the number of series RL-pairs originating from the center of the patch is equal to n. The coupling

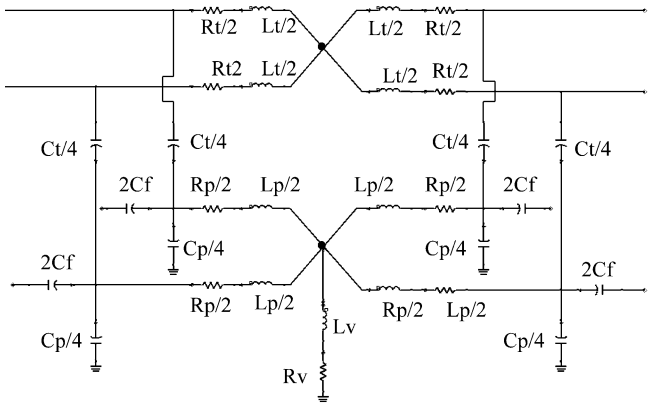

Fig. 19. Compact model of power plane unit cell. Resistive losses are included. Parameters are given as function of total capacitance ($\mathrm{Ct} = 0.96$ pF, $\mathrm{Cp} = 0.91$ pF, $\mathrm{Cf} = 0.47$ pF), total inductance ($\mathrm{Lt} = 1.14$ nH, $\mathrm{Lp} = 5$ pH, $\mathrm{Lv} = 0.81$ nH) and total resistance ($\mathrm{Rt} = 0.38\varsigma$, $\mathrm{Rp} = 0.18\varsigma$, $\mathrm{Rv} = 0.26\varsigma$).

capacitors to ground and to adjacent patches are available on each size of the unit cell.

B. Compact Model Extraction

The extraction of the compact model involves the following steps: First, S-parameters are generated for a system of two-unit cells using electromagnetic full wave simulation. Second, initial values are assigned to the model form using existing formulas for thin film inductors and parallel-plate waveguides described in [17] and [28], and a circuit analysis tool such as Agilent ADS [29] is used to extract the values of the model components by fitting the simulated S-parameters against that of the model. The final model of a full-size power plane is then obtained by connecting several of the unit cell models into a two-dimensional array.

To validate the model, we considerer two power planes denoted as power plane 1 and power plane 2. Power plane 1 measures 9×10 cm and has a HIS with 1.54-mm-high vias and square patches with period of 1 cm. The separation between the patches is 400 μm and the distance between the HIS and the V_{dd} plane is 1 mm. Power plane 2 measures 10×10 cm and has an inductance-enhanced HIS employing a single-loop inductive element of length 16 mm. The total thickness of the power plane (including HIS) is 1.54 mm and the spacing between the patches is 400 μm.

Fig. 20 shows a comparison between insertion loss obtained using the three-dimensional full-wave simulation using HFSS and the compact circuit model for power plane 1. The noise source (port 1) is located at (4.5 cm, 4.5 cm) and the load (port 2) is located at (4.5 cm, 1.5 cm). A good match is obtained over the frequency range of interest.

Fig. 21 shows the modeled (using HFSS) versus simulated (compact circuit model) insertion loss (S12) of power plane 2. Port 1 and port 2 are located at (4.5 cm, 4.5 cm) and (4.5 cm, 1.5 cm), respectively. A good match is obtained from DC up to the upper edge of the stopband. Above this upper corner frequency, the two curves have the same shape, with a frequency (phase) shift of about 0.4 GHz between simulation and modeling. This

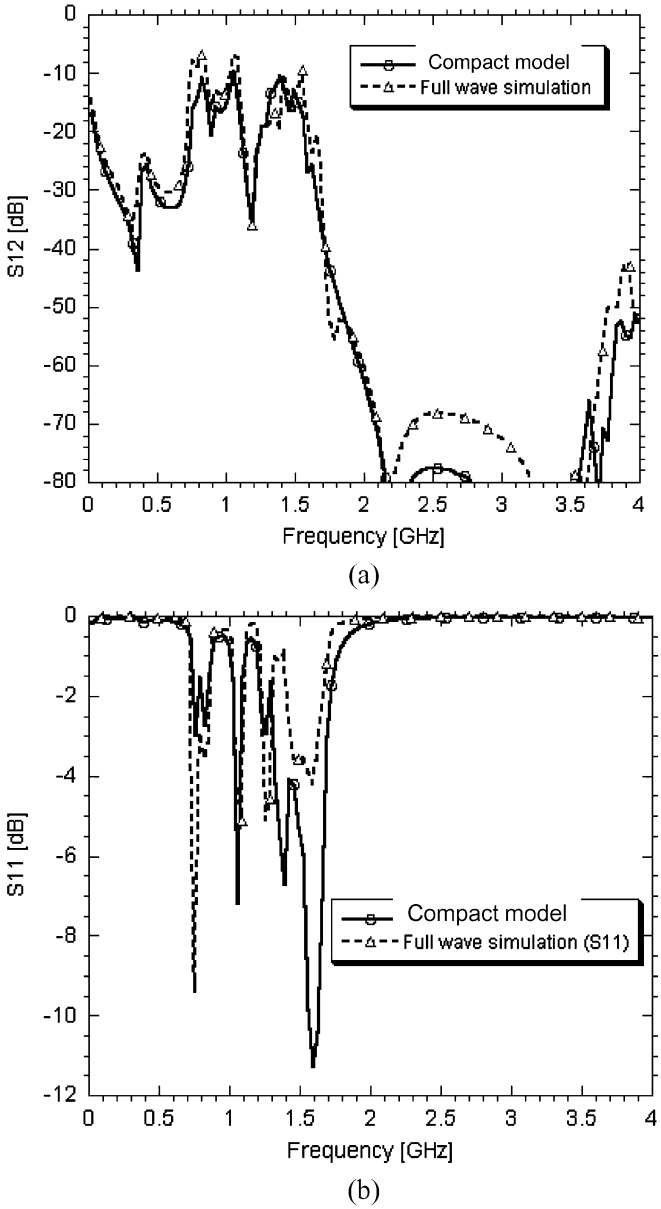

Fig. 20. Modeled versus simulated magnitude of S-parameters for power plane 1: (a) S12 and (b) S11.

discrepancy can be adjusted by additional tuning of the model component values; however, this discrepancy is insignificant as the primary objective of the model is to predict the stopband behavior.

For a 10×10 cm power plane, the total simulation required to run the compact model is less than 10 s. The full-wave three-dimensional simulation using HFSS, on the other hand, requires approximately 40 h.

VI. Compact Model Application

A. Noise Mitigation at Different Locations on the Power Plane

The compact model defined above can now be used in a circuit simulator for the analysis of the noise mitigation capability of the power plane system. Since the model is physics

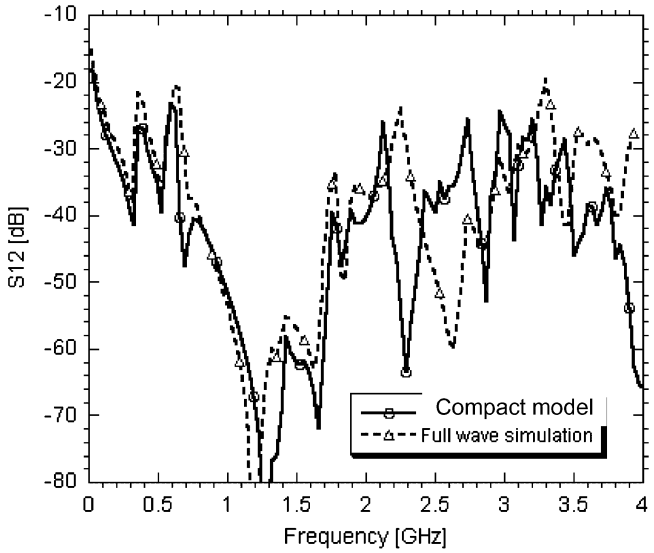

Fig. 21. Modeled versus simulated insertion loss of power plane 2.

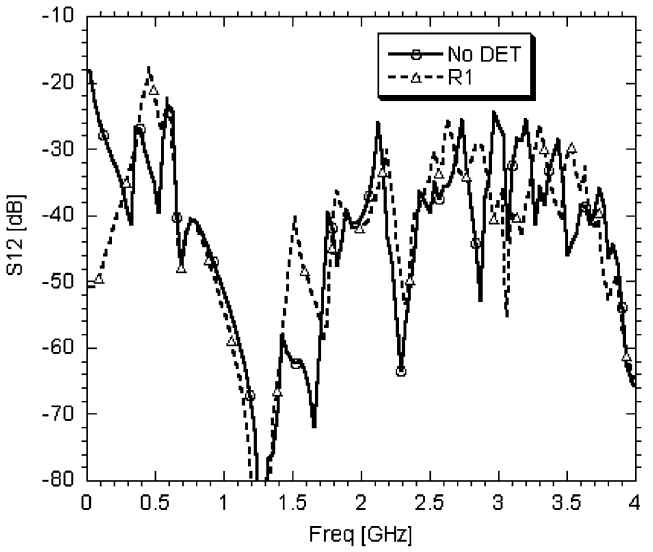

Fig. 23. Insertion loss of the power plane 2 with and without RC dissipative edge termination, R $= 1\ \Omega$.

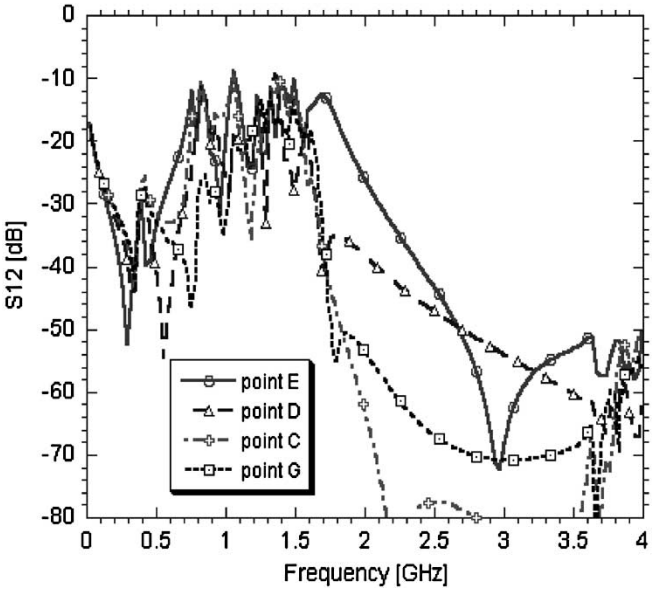

Fig. 22. Insertion loss of power plane 1 for different noise source to load distances.

based and periodic, its validity is not restricted to the position of the load and noise sources as defined in the reference full-wave simulation used to extract the model component values.

To study the position dependency of the noise mitigation we considered plane 1. First, the noise source (port 1) was fixed at point A (4.5 cm, 4.5 cm) and the load was moved through the points E-D-G-C of coordinates (4.5 cm, 3.5 cm), (4.5 cm, 2.5 cm), (4.5 cm, 1.5 cm), and (4.5 cm, 0.5 cm), respectively. The resulting insertion loss (S12) is plotted in Fig. 22. When the receiving port (load) is closest to the noise source, the absolute bandwidth is minimal. As the distance increases, the bandwidth saturates. In general, band-gap width saturation is reached when the noise source and the load are at least two periods from each other.

B. Combination of HIS With Decoupling Capacitors

Resonance in parallel-plate power planes (waveguides) with finite width is usually due to the in-phase addition of incident and reflected waves, which results in standing waves. To mitigate those resonances, *RC* dissipative edge termination (DET) can be placed between the $V_{\rm dd}$ and the ground plane at the edges of the board as reported in [30] and [31]. This technique is applicable to both traditional power planes and power planes with integrated HIS. Fig. 23 shows the insertion loss of power plane 2 with and without decoupling capacitors. A substantial attenuation of the transmission coefficient is achieved at very low frequencies with decoupling capacitors. Here each decoupling capacitor is modeled as a series *RLC*, with C being the desired decoupling capacitance, L the associated lead inductance, and R a resistance (generally) selected to match the impedance of the parallel plate waveguide without HIS [31].

Unlike for regular parallel-plate waveguides, there are no established formulas for the impedance of parallel-plate waveguide with integrated HIS. To determine the optimum value of R for broadband SSN mitigation, 40 decoupling capacitors (*RLC*) connecting the $V_{\rm dd}$ and the ground planes were placed around the perimeter of power plane 2. With L and C fixed at 0.5 nH and 1 nF respectively, the resistance R was varied from 5 to 40 Ω. As illustrated in the insertion loss plot of Fig. 24, the resonant mode attenuation improves at high frequencies as R increases, but at the same time there is a small degradation of the resonant mode mitigation at low frequencies. For a value of R too large, there is no mitigation due to the DET since $R > 1\ \omega C$ at all frequencies. For the case considered here, a resistance value of 20 Ω provides reasonable noise mitigation at DC and also minimizes the high-resonant mode transmission seen around 600 MHz.

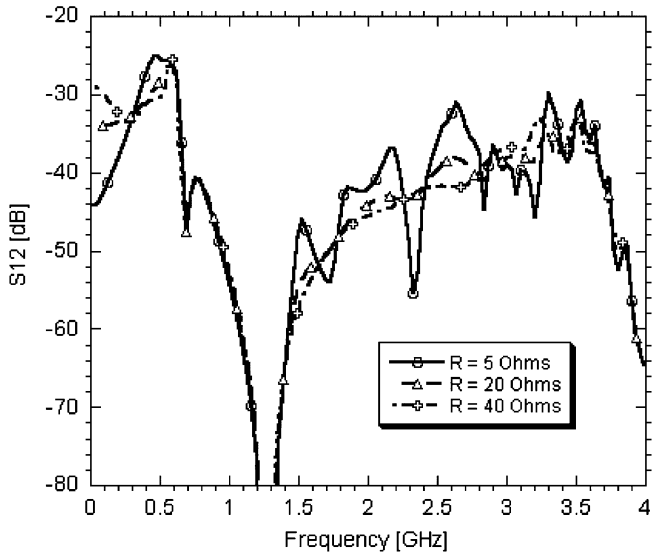

Fig. 24. Effect of shunt resistance on high-frequency noise mitigation.

VII. Conclusion

The application of high-impedance electromagnetic surfaces for SSN mitigation in power planes has been investigated. This novel concept has the potential of suppressing parallel-plate modes in the frequency range where the HIS has its forbidden bandgap. Full-wave simulation was used to show that a careful design of the HIS would provide broadband noise mitigation in most frequency ranges of interest for today's computer systems. Inductance-enhanced HIS using single-loop or spiral inductors can provide broadband noise mitigation at frequencies below 1 GHz while maintaining a reasonable thickness for the power plane system. This is a significant advantage over the standard HIS where the inductance enhancement is obtained by increasing the via height and therefore the thickness and weight of the power plane. A lumped-element compact model has been developed for these novel power planes. The compact model is based on the unit cell approach and can be expanded to model power planes with different sizes and single or multiple layers. The model was validated on power planes with simple and inductance-enhanced HIS. Good match was obtained between the modeled and the simulated S-parameters over the frequency range of interest. The compact model offers a significant cost advantage to the full-wave simulation as it reduces the simulation time of a typical 10×10 cm power plane from approximately 40 h to less than 70 s on the same workstation. It was also demonstrated that the HIS provides azimuthal noise mitigation over the entire power plane. In addition, its combination with decoupling *RC* networks provides broadband noise mitigation from DC to the upper edge of the HIS forbidden bandgap.

Finally, we emphasize that the objective of this work was not only to show a faster way for analyzing power planes, but also to demonstrate that once a compact model has been extracted, it can be used in combination with models of other package elements such as resistors and capacitors to provide a fast analysis of the high-speed package. The reuse of such a model is more efficient than running full-wave analysis every time a new component is added to the package.

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