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POWER-AMPLIFIER DESIGN USING NEGATIVE-IMAGE DEVICE MODELS

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ABSTRACT: A novel design methodology for wireless power amplifiers is presented using negative-image device models that are applicable to GaAs FETs and other power devices. Negative-image device models of a power device are generated by incorporating hypothetical negative-image matching networks and a load-line theory with optimization technique. The negative-image device-modeling methodology provides the following advantages in comparison to previously developed techniques: (i) it can predict achievable amplifier performance in the device-modeling stage; (ii) it provides an accurate starting point for the synthesis of impedance-matching networks; (iii) it can make use of widely available linear simulators. Descriptions of the negative-image device-modeling method and its application to the design of a high-power GaAs FET amplifier are presented. The experimental results of an implemented amplifier are given as a demonstration of the effectiveness of the proposed design methodology. © 2005 Wiley Periodicals, Inc. Microwave Opt Technol Lett 47: 197–201, 2005; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.21122

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1. INTRODUCTION

Increasing demand and market trends for high-power amplifiers require designers to obtain optimum performance from power devices, and predict obtainable circuit performance in the beginning stage of a circuit design. A traditional key requirement for power amplifiers is to extract maximum output power with high efficiency from power devices. With the development of multicarrier communication systems, nonlinear characteristics of power amplifiers are becoming more critical parameters in the evaluation of power amplifiers. Since the power amplifier is one of the most critical components with regard to system performance and cost,
engineers are increasingly challenged to extract optimal performance from cost-competitive devices [1].

Several techniques have been developed in the past to aid in building wireless power amplifiers with required performance. In [2, 3], a load-line method for power transistors has been introduced to determine optimum load resistance for maximum output power. When used with small-signal-device equivalent circuits, the method is generally recognized as a good design technique for wireless power amplifiers. The load-line method is typically used for the design of hybrid power amplifiers because some tuning procedures are needed to achieve the desired performance. In [4–7], a load-pull technique has been developed to evaluate the performance of power devices in terms of output power, power-added efficiency, and intermodulation. This technique is, however, difficult to implement, and requires considerable time to characterize a single device. The measurements have also several limitations due to potential device oscillation, inherent tuner loss, and damage possibility for highly mismatched loads. In [8–11], device-modeling techniques for nonlinear computer-aided design (CAD) programs have been introduced. In spite of their advantages for power-amplifier design, the extraction of nonlinear device models is cumbersome, since it involves measurements of small-signal \( S \)-parameters at various bias points. Nonlinear device models are not usually provided by device manufacturers, but small-signal \( S \)-parameters at DC bias points and DC \( I-V \) characteristic curves of devices are typically given.

In this paper, we introduce a design methodology for wireless power amplifiers using a negative-image device-modeling method for power devices. Negative-image device models of power devices are generated by a negative-image amplifier model that uses the small-signal \( S \)-parameters of a power device, a load-line method, and computer optimizations. The negative-image modeling methodology provides following advantages over the previous methodologies mentioned above:

1. it can predict amplifier performance from power devices without nonlinear device models;
2. it can generate two-element device models that provide accurate and highly convenient starting point for matching network synthesis;
3. it can make use of widely available linear simulators that have high accessibility to most circuit designers.

In section 2 of this paper, a methodology for deriving negative-image device models of power devices is described for power amplifier applications. In section 3, negative-image device models for a practical power GaAs FET are derived, and a design example of an L-band power amplifier is given using derived device models and distributed matching-network synthesis. In section 4, the discussion about the proposed methodology for a power amplifier design is presented.

2. NEGATIVE-IMAGE DEVICE MODELS

Negative-image device models were first introduced for the design of wireless small-signal amplifiers in [12, 13]. The method can accurately predict small-signal circuit performance in device-modeling stage, because device models generated using this method can reflect desired circuit performance by a computer optimization. If a maximum-power transfer condition is incorporated into small-signal negative-image models, we can generate large-signal negative-image device models of power devices from the theory of small-signal negative-image models. Since such device models are usually represented as simple two-element models with a resistor and reactive element, large-signal negative-image device models provide an accurate starting point for matching network synthesis of power amplifiers. In this section, the generation of large-signal negative-image device models for power devices is described using negative-image matching networks, small-signal \( S \)-parameters, and DC \( I-V \) characteristics of power devices.

A network for generating large-signal negative-image device models is shown in Figure 1. It consists of a power device with measured small-signal data and negative-image input and output matching networks. Assuming the input and output device models of a power device are given for desired amplifier performance, the hypothetical input and output matching circuits in Figure 1, which exactly match the given models at all frequencies, can be generated as mirror images of the device models with model element values that are replaced by corresponding negative values. Therefore, each negative-image matching network contains hypothetical lumped or distributed elements with negative element values.

If we use the \( ABCD \) matrix in the \( S \)-plane (\( S \) is the complex frequency variable for lumped elements and the Richards variable for distributed elements), it can be shown that the negative-image input and output circuits in Figure 1 provide the required matching. Since the multiplication of two matrices which correspond to the positive element for the device model and the adjacent negative element for the negative-image circuit in each cascaded network is equal to the identity matrix, the corresponding positive and negative elements can be removed from the cascaded network. After such elimination, the remaining adjacent positive and negative elements are again repeatedly removed until two terminating resistances finally remain in each cascaded circuit, which proves that \( ABCD \) matrix between two terminating resistances is the unity matrix. Therefore, the cascade of input or output device model with its corresponding negative-image network in Figure 1 results in an identity matrix, indicating that such negative-image networks give the required matching at all frequencies.

In practical power-amplifier design, large-signal input and output device models of power devices, such as power GaAs FETs, are not usually given to designers, but have to be determined for a specified performance. The required device models can be generated by the inverse of the above-mentioned procedure using output-power requirements, small-signal device data, and DC \( I-V \) characteristics of power devices. First, in order to build large-signal negative-image device models, topologies, and initial element values, negative-image matching networks have to be determined from the conditions of maximum output power and desired small-signal performance. In the hypothetical output circuit shown in Figure 1, the impedance that must be presented to the device or the impedance seen into the negative-image network has the following optimum load resistance for maximum output power [14, 15]:

\[
R_{opt} = \left( \frac{V_{DS}^{\max} - V_t}{2I_{D1}} \right),
\]
where $V_{DS\,\text{max}}$ and $I_D\,\text{max}$ are the maximum drain-source voltage and drain current in a power transistor, respectively. In Eqs. (1) and (2), $V_\alpha$ is a knee voltage and $I_{D1}$ is a fundamental component of the drain current. The angle $\alpha$ is a conduction angle. In the actual device, the resistance of $R_{OPT}$ is transformed into frequency-dependent optimum impedance due to the device output capacitance, bond-wire inductance, and package parasitics, which can usually be calculated by the measured small-signal $S$-parameters of a device. Optimum load reactance, which should be presented to the device by the negative-image output network, is initially set to cancel out the output reactance of a device calculated from $S_{22}$. Thus, the topology and element values of the hypothetical output circuit can be deduced from the optimum load resistance and $S_{22}^*$ loci of a device on the Smith chart. On the other hand, the topology and element values of a hypothetical input network are determined from source mismatch gain circles on the Smith chart, so that the impedance seen into the negative-image input circuit provides the required amplifier performances, such as gain and return losses.

Next, the hypothetical input and output matching networks are cascaded with a power device characterized by small-signal $S$-parameters and DC I–V curves, as shown in Figure 1, and then a computer optimization is applied to the combined structure for a specified performance. In the optimization, the optimization parameters are the element values of the hypothetical negative-image input and output circuits, and the optimization results are a pair of optimized hypothetical networks that satisfy the required amplifier performance. Finally, we obtain a large-signal device input model by the negative-image looking to the left at plane 1 in Figure 1 and a large-signal device output model by the negative-image looking to the right at plane 2, which provide desired amplifier performance. For maximum output power, the optimum load reactance in the output matching network is maintained with the value calculated from Eqs. (1) and (2) during optimization. Since the output capacitance of a power transistor is not strongly dependent on the high-frequency input signal level [15, 16], large-signal negative-image device models in this paper, which use small-signal $S$-parameters for the calculation of device reactance, are well suited for the design of wireless power amplifiers.

### 3. DESIGN EXAMPLE

The design of a 1.4–1.5-GHz power amplifier is presented to illustrate the device-modeling methodology in the previous section and its application to the design of wireless power amplifiers. The Fujitsu high-power GaAs FET, FLL57MK, which is biased for a class AB operation, was chosen, because detailed data (output power, PAE, DC I–V characteristics, and small-signal $S$-parameters) are available. The design specifications will be the output power of 4 W at the 1-dB gain-compression point, power-added efficiency (PAE) of 37%, and small-signal power gain of 13.5 dB across the operating-frequency range.

#### 3.1. Negative-Image Device Models

Circuit topologies of negative-image input and output networks can be determined from source mismatch gain circles on the Smith chart and the measured $S_{22}$ loci of the FLL57MK, respectively. For a negative-image output circuit, a series topology is chosen from the $S_{22}$ of the device over the operating-frequency range. Since the output reactance of the device increases with frequency over the same bandwidth, the reactance of negative-image output network, looking into the right at plane 2 in Figure 1, should decrease with frequency so as to cancel out the device output reactance. Therefore, the negative-image output circuit becomes a series combination of a resistor with an optimum load resistance and a capacitor with a negative capacitance. The optimum resistance and initial capacitance value are calculated as 7.8Ω and $-110\,\text{pF}$ from Eqs. (1) and (2) and the measured $S_{22}$, respectively. The hypothetical output network provides the operating power gain of 15.5 dB at the center operating frequency. On the other hand, a negative-image input circuit needs to provide a mismatch of 2.0 dB in order to achieve an overall power gain of 13.5 dB. From the source-mismatch gain circles over the operating frequency bandwidth, a series topology with a resistor and a capacitor with negative capacitance is chosen for a hypothetical input network. Its initial resistance and capacitance values are calculated as 11.6Ω and $-31.5\,\text{pF}$, respectively. A schematic representation of a negative-image amplifier model, shown in Figure 2, is combined with the FLL57MK and negative-image input and output matching circuits.

Next, the negative-image amplifier model in Figure 2 is optimized to achieve the desired amplifier performance. The optimized amplifier model and its responses are shown in Figures 2 and 3, respectively. The desired negative-image device models are derived by taking negative images for optimized hypothetical matching networks, as shown in Figure 4. The input and output device models predict that a power amplifier using these models will provide output power of 4 W, PAE of 37% at 1-dB gain compression, and the optimized small-signal performance presented in Figure 3. The output power and PAE are referenced by the manufacturer’s device data sheet. The optimized performance of an
ideal negative-image amplifier model exhibits the gain of $13.5 \pm 0.35$ dB, and minimum input and output return losses of 3.8 and 16.3 dB, respectively.

3.2. Impedance-Matching Networks

Since both input and output device models in subsection 3.1 contain a series capacitor, it is necessary to design impedance-matching circuits in the form of high-pass or band-pass structures. For band-pass networks, however, it is difficult to obtain circuits that exactly absorb both the capacitance and resistance of device models, and high-pass networks can bring about stability problems in the lower-frequency region. Thus, we use quasi-low-pass networks suitable for exact parasitic absorption and harmonic termination as matching circuits. Distributed impedance-matching networks are used to match the negative-image input and output device models in Figure 4.

The power gain of a quasi-low-pass distributed network that consists of commensurate transmission lines is given by [17, 18]:

$$|S_2|^2 = \frac{K}{1 + (e^4/2)[1 + \cos(n\phi + r\xi)]}, \tag{3}$$

where $n$ and $r$ are the number of transmission-line elements (TLE) and low-pass elements, respectively. The power gain of Eq. (3) exhibits equal ripple characteristics. $K$ and $e$ are a gain and ripple parameter of the network. The network order of $n + r$ must be an even number. The expressions for $\phi$ and $\xi$ are given by

$$\cos \phi = \frac{\Omega^2(\Omega_1^2 + \Omega_2^2 + 2) - (\Omega_1 + \Omega_2)^2}{(\Omega_2 - \Omega_1)^2(1 + \Omega^2)}, \tag{4}$$

$$\tan \theta = \tan \beta l, \quad \Omega_1 = \tan \theta_1, \quad \Omega_2 = \tan \theta_2.$$

Angles of $\theta_1$ and $\theta_2$ are electrical lengths of transmission lines at lower and upper band-edge frequencies, respectively. An impedance function corresponding to Eq. (3) is derived using the unitary condition for a lossless network and the following formula:

$$z(S) = \frac{1 + S_{11}(S)}{1 - S_{11}(S)}, \tag{6}$$

where $S_{11}(S)$ is the input reflection coefficient and $z(S)$ is the normalized input impedance of the circuit. The Richards variable of $S$ is equal to $\Sigma + j\Omega$. If the electrical length of the distributed elements, gain, and ripple parameters are properly chosen, we can synthesize the distributed networks for matching the input and output device models using Eqs. (3)-(6).

In this study, we choose the network order of $n = r = 2$, considering the operating-frequency bandwidth. The input and output matching networks, which are synthesized to contain device models as a part of the networks, are given in Figure 4. The input matching network is synthesized by setting the minimum insertion loss (MIL) as 0 dB, ripple as $1.95 \cdot 10^{-5}$ dB, and electrical length as $\theta_2 = 35^\circ$, and the output matching network by choosing MIL as 0 dB, ripple as $3.55 \cdot 10^{-5}$ dB, and electrical length as $\theta_2 = 35^\circ$ over the operating-frequency range. The capacitors of the device models can be exactly absorbed by adjusting the length of TLEs adjacent to device model resistances in Figure 4. TLEs of 25.8\Omega

Figure 5 Schematic of an optimized power amplifier

$$\cos \xi = \frac{2\Omega^2 - (\Omega_1^2 + \Omega_2^2)}{(\Omega_2^2 - \Omega_1^2)}, \tag{5}$$

where $\Omega = \tan \theta = \tan \beta l, \, \Omega_1 = \tan \theta_1, \, \text{and} \, \Omega_2 = \tan \theta_2$. The power gain of Eq. (3) is equal to $\Sigma + j\Omega$. If the electrical length of the distributed elements, gain, and ripple parameters are properly chosen, we can synthesize the distributed networks for matching the input and output device models using Eqs. (3)-(6).
mirror images of the optimized negative-image matching circuits. Negative-image device models for a power device are derived by taking minimization techniques for specified circuit performance, and negative-image modeling methodology presents a viable alternative when designing power amplifiers in the absence of nonlinear device models of power devices.

3.3. Amplifier Performance
The power amplifier constructed by the combination of the device models and matching networks is shown in Figure 5. The amplifier has been optimized for flat gain and practical realization. Shorted quarter-wavelength shunt stubs at the center frequency are added to provide bias injection and even harmonic termination in the input and output matching networks. Figure 6 shows calculated small-signal responses of the optimized amplifier using a linear circuit simulator. The power gain from this design is 13.5 ± 0.05 dB over the operating-frequency bandwidth. The input and output return losses are better than 3.5 and 14.2 dB across the same frequency range, respectively. The predicted output power and PAE are 4 W and 37% at the 1-dB gain compression point, respectively.

The designed amplifier has been implemented using microstrip lines on the 30-mil microwave substrate with the dielectric constant of 4.2. Figures 6 and 7 show the measured small- and large-signal responses of the power amplifier. The power gain is 13.1 ± 0.08 dB over the operating-frequency range. The input and output return losses are better than 2.4 and 14.4 dB over the same frequency bandwidth, respectively. The output power is more than 3.72 W, and PAE is better than 35.1% at the 1-dB gain compression point. The measured results show good agreement with the predicted performance of the power amplifier.

4. CONCLUSION
A novel design methodology for wireless power amplifiers using negative-image device models has been introduced. Negative-image device models of power devices, which provide the desired amplifier performance, are generated using a negative-image amplifier model that makes use of hypothetical negative-image matching networks and device data supplied by most device manufacturers. The negative-image amplifier model incorporates optimization techniques for specified circuit performance, and negative-image device models for a power device are derived by taking mirror images of the optimized negative-image matching circuits.

A design example of an L-band power amplifier was presented with the distributed matching-network synthesis in order to demonstrate the effectiveness of the design approach using negative-image device models. The measured results of the implemented amplifier are in good agreement with the predicted results. The negative-image modeling methodology presents a viable alternative when designing power amplifiers in the absence of nonlinear device models of power devices.

REFERENCES

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